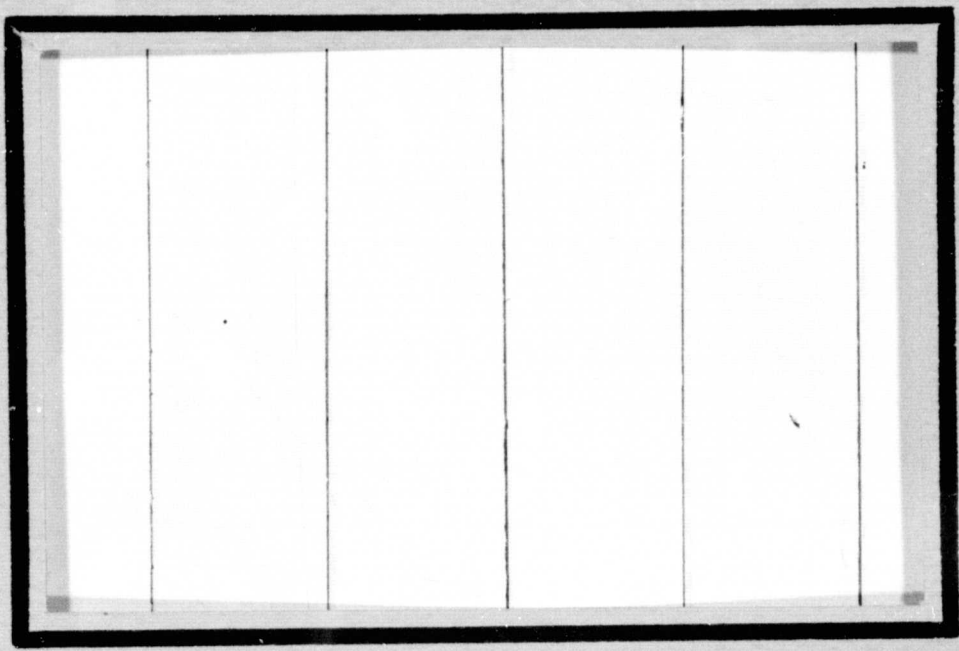


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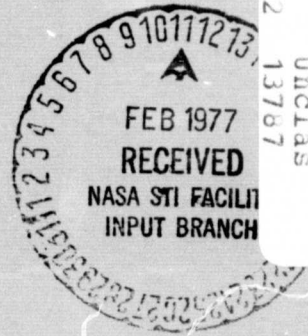
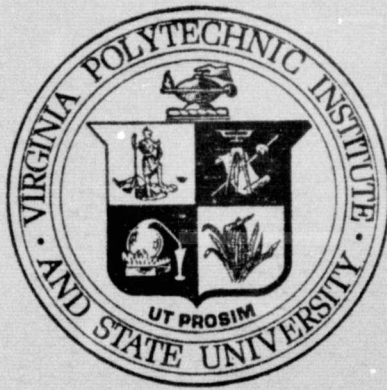
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Final Report (First Year of Work)

on

A DEPOLARIZATION AND ATTENUATION EXPERIMENT
USING THE CTS SATELLITE

Volume 1. Experiment Description

by

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1. Introduction

1.1 Purposes of the Experiment

The VPI&SU CTS Experiment is concerned with precipitation depolarization and attenuation on satellite downlinks at 11.7 GHz. It is motivated by a growing world-wide need for more domestic and international satellite communication channels, a need that can be met only by expansion into vacant allocations above 10 GHz. The goals of the experiment are (1) to monitor attenuation and depolarization of the signal received from the spacecraft on a fully automated 24-hour basis, (2) to correlate these with ground weather conditions, (3) to refine existing theoretical models for millimeter wave propagation through rain for maximum agreement with observed data, and (4) to develop techniques for predicting and minimizing the effects of rain scatter and depolarization on future satellite communications systems.

1.2 Experiment Description and Terminology

The CTS spacecraft transmits an 11.7 GHz beacon signal that is nominally right-hand circularly polarized (RHCP). Technically the transmitted signal is right-hand elliptically polarized (RHEP), and as such it may be represented as the superposition of a relatively large RHCP wave and a relatively small LHCP wave. If we call the electric field amplitudes associated with these component waves E_{RHCP} and E_{LHCP} respectively, then the polarization purity of the wave may be described by the cross polarization ratio or CPR where

$$\text{CPR (in dB)} = 20 \log_{10} \frac{|E_{\text{LHCP}}|}{|E_{\text{RHCP}}|} . \quad (1)$$

With this definition, a pure RHCP wave would have a CPR of negative infinity decibels.

When the downcoming wave from the satellite interacts with precipitation or high-altitude ice crystals, a small amount of energy is coupled from the RHCP component to the LHCP component. This raises the CPR and in a communications system (like the proposed Intelsat V) which uses orthogonal polarization to transmit two message channels on the same frequency it would also raise the crosstalk level.

At the VPI&SU earth station a dual polarized receiving antenna separates the RHCP and LHCP components of the received signal and routes them to separate receiver channels. These are called the co-polarized and cross-polarized channels, respectively, and the corresponding antenna output ports are called the co-polarized and the cross-polarized ports.

Since the spacecraft is transmitting one polarization (as opposed to two orthogonal polarizations in an orthogonal polarization frequency sharing communications system), the isolation between the channels is the ratio of the received power in the co-polarized channel to the received power in the cross-polarized channel. Thus, at the receiving antenna output

$$I \text{ (in dB)} = 10 \log_{10} \left[\frac{\text{power output from the co-polarized port}}{\text{power output from the cross-polarized port}} \right] \quad (2)$$

In practice the receiving antenna is not perfect, and a small but unavoidable amount of coupling exists between the LHCP component of the received signal and the co-polarized port of the antenna. A similar coupling

is present between the cross-polarized port and the RHCP component of the incoming wave. This coupling keeps the isolation finite even under clear weather conditions. Any depolarization in the atmosphere reduces the isolation and under severe conditions the isolation in dB approaches the magnitude of the CPR in dB.

Amplitude detectors in the VPI&SU receiving system automatically monitor the power levels of the incoming co-polarized and cross-polarized signal components. When one of these changes by 0.8 dB its new value is stored by a Digital Equipment Corporation PDP-11/10 computer system for later processing. The system isolation and any rain or atmospheric attenuation are calculated from these data. The relative phase angle between the co and cross-polarized signal components is also recorded.

Simultaneous ground weather information is collected by a network of 5 rain gauges, 2 wind sensors, and one thermometer. These instruments are backed up by a 15 GHz weather search radar which provides a visual indication of weather conditions along the path. Figure 1.1 shows the locations of the weather instruments.

In the following sections of this report each subsystem of the VPI&SU experiment is described in detail. To help the reader visualize the roles and appearance of the various components, Figure 1.2 shows the overall receiving and data collection system. Figures 1.3 through 1.6 illustrate the antenna and RF front end. These pictures were made by the University to publicize the CTS experiment and show two electrical engineering students operating the equipment.

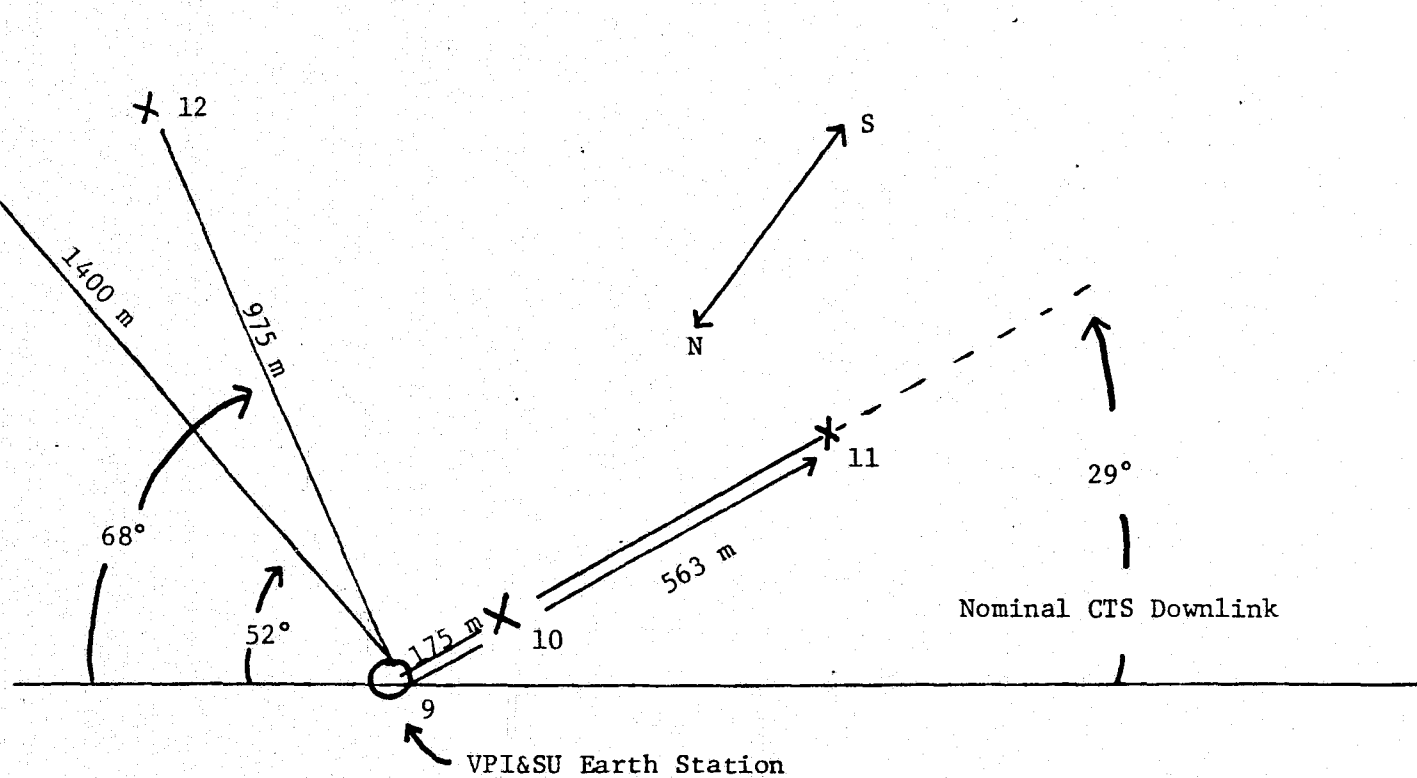


Figure 1.1. Location of rain gauges with data numbers 9 through 13.
Wind sensors are located at 9 and 10.

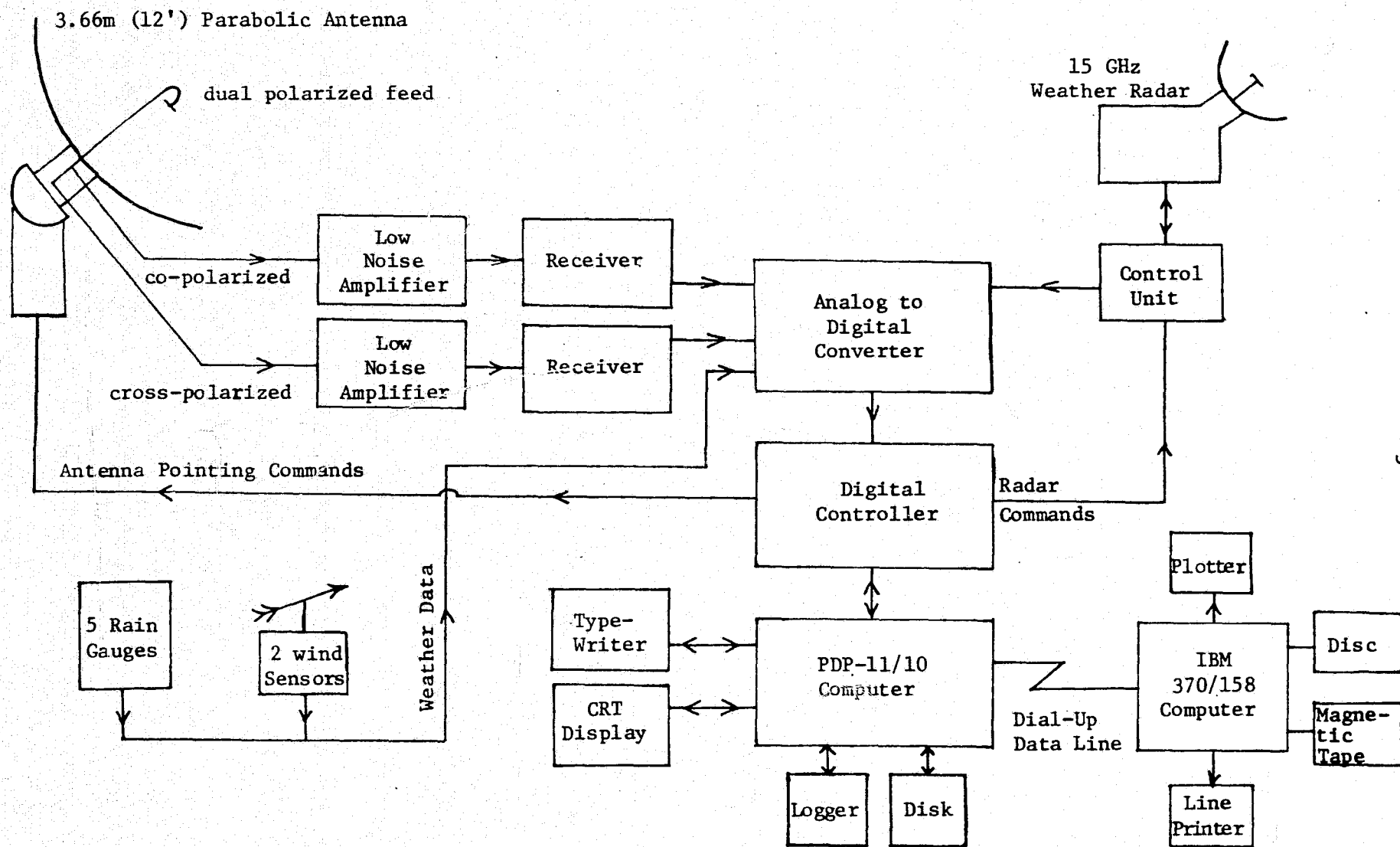
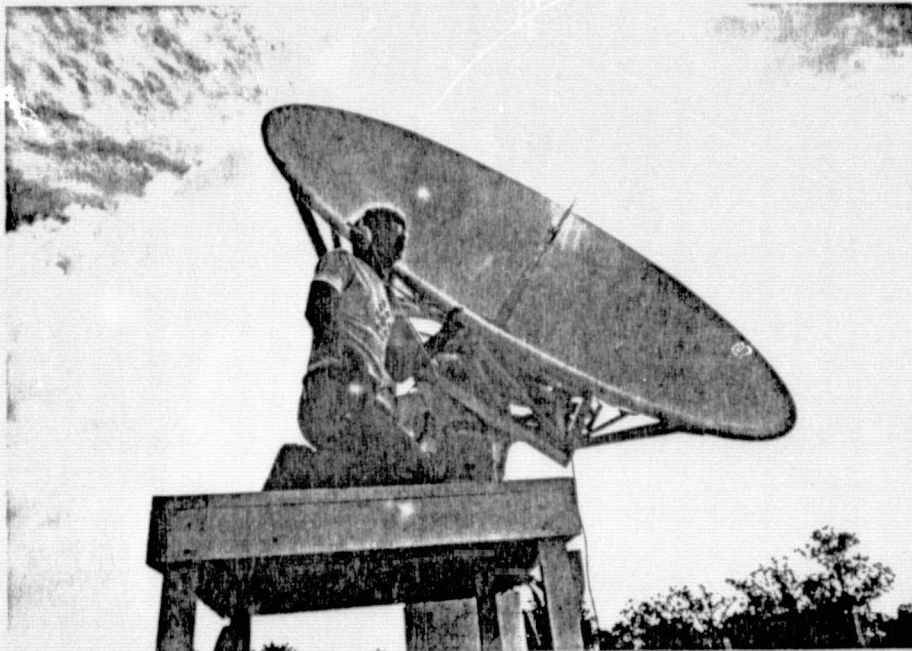
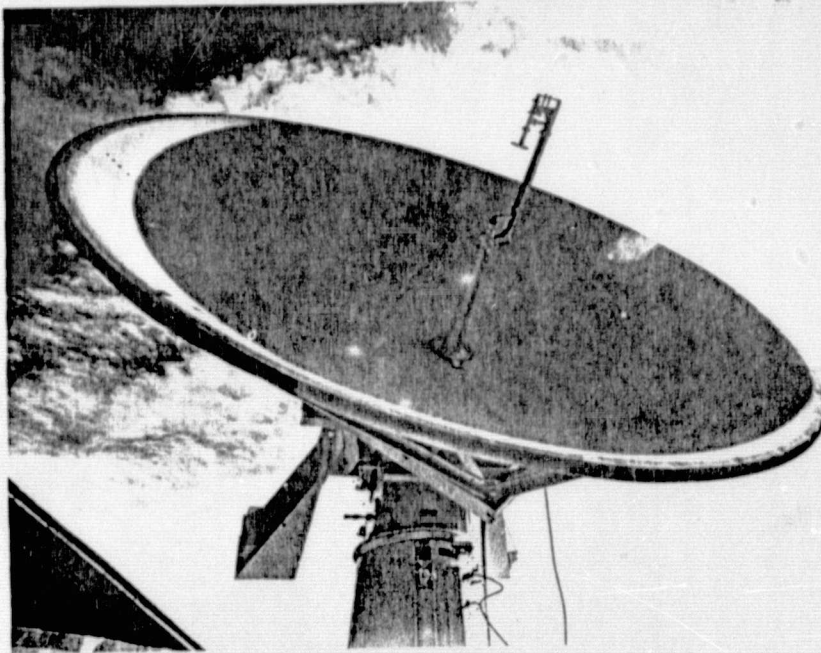


Figure 1.2 System block diagram.



Figures 1.3 and 1.4. CTS Receiving Antenna

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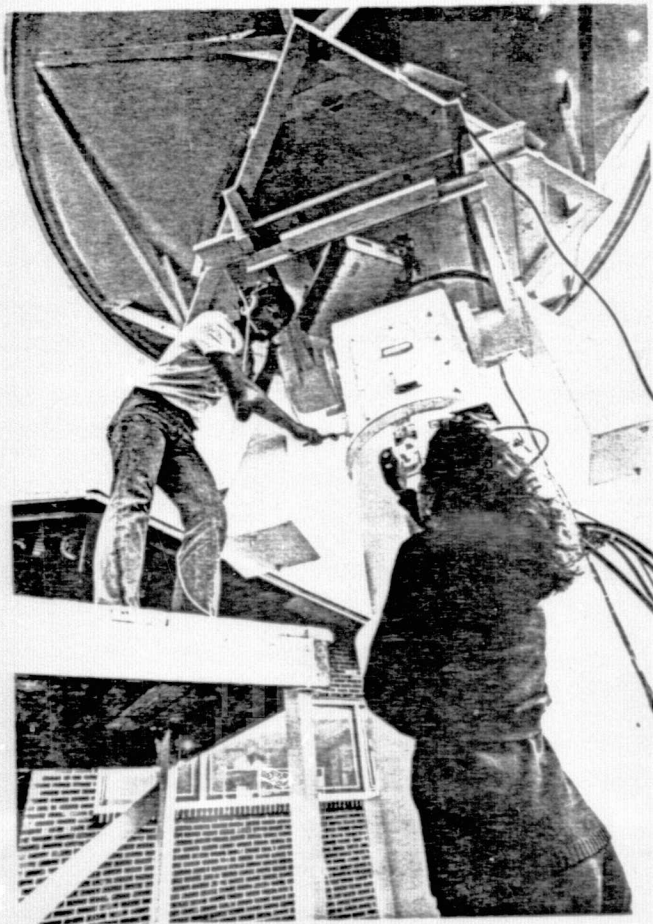


Figure 1.5 Antenna Pedestal and RF Front End

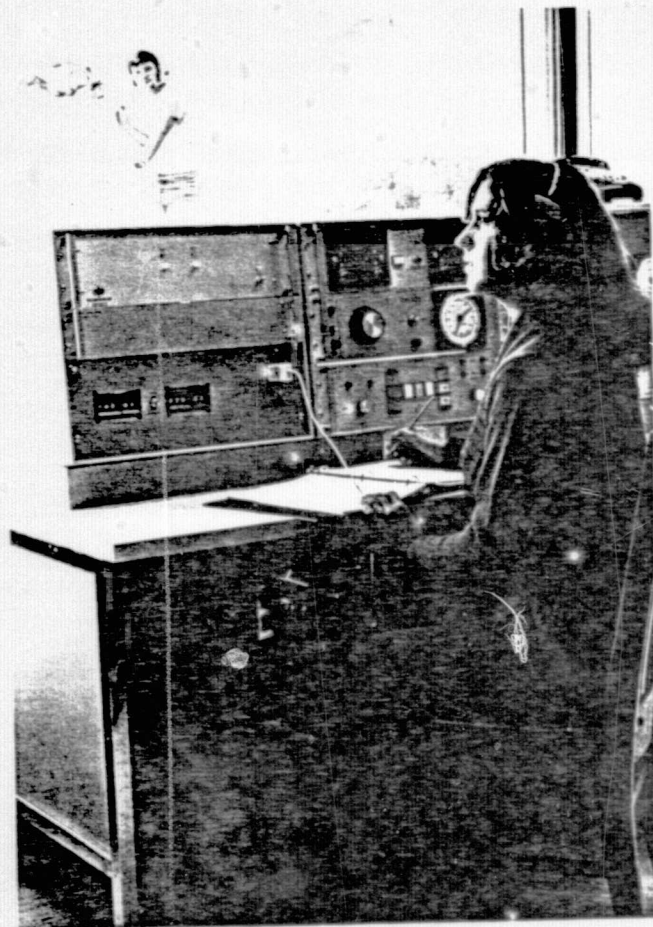


Figure 1.6. Antenna Console

2. The Antenna System

2.1 Description

The VPI&SU CTS receiving antenna shown in Figure 2.1 is a Scientific Atlanta 3.66 meter (12 foot) diameter parabolic reflector with a dual-polarized prime focus feed system. While the antenna was designed for optimum performance at the 11.7 GHz beacon frequency, it will cover the CTS transponder frequencies as well.

A prime focus design was selected instead of a Cassegrain system to avoid water droplet formation on the feed horn. This does not occur in a prime focus system because the feed horn normally points down and its aperture is protected from the rain.

The feed used in the antenna is a wide-angle multimode corrugated horn which provides a circularly symmetric pattern as well as high aperture efficiency, low aperture blockage, and very good sidelobe suppression. The horn may be rotated by hand to provide either dual linear or dual circular polarization.

Following the feed horn are an orthomode transducer and a tapered waveguide section. There are two waveguide outputs from orthomode transducer-taper combination. The output from each waveguide represents an orthogonal component of the wave incident on the antenna. These waveguides are formed into a "button hook" and pass through the apex of the dish. The feed assembly has no support spars. At the apex of the dish a roller bearing complex provides for manual rotation of the entire feed about the axis of the horn. The RF front ends for both channels are also attached to the feed assembly on the rear of the reflector and rotate with the feed. Flexible

coaxial cable outputs at the IF frequency (1.05 GHz) allow 360° rotation.

At first glance it may appear unnecessary to rotate the feed system of a circularly polarized antenna. This would be true if either the transmitting or the receiving antenna were perfectly circular. Since both are actually elliptically polarized, rotating the feed aligns the major axes of the polarization ellipse of the incoming wave with those of the receiving antenna and thereby minimizes the polarization mismatch and maximizes the cross polarization isolation. A quantitative discussion of this point follows in Section 2.3.

2.2 Antenna Specifications

Table 2.1 lists the specifications and test data for the antenna.

2.3 Expected Antenna Performance

2.3.1 General Considerations

The output power available from an antenna receiving an incident wave of flux density S is given by

$$W = m_p S A_e \quad (1)$$

where

S = flux density of incoming wave [watts/m²]

A_e = effective aperture of the antenna [m²]

m_p = polarization mismatch factor between the polarization state of the wave and the antenna

There are many formulations for m_p which are discussed in many texts. For the moment we will represent it as a function of the polarization state

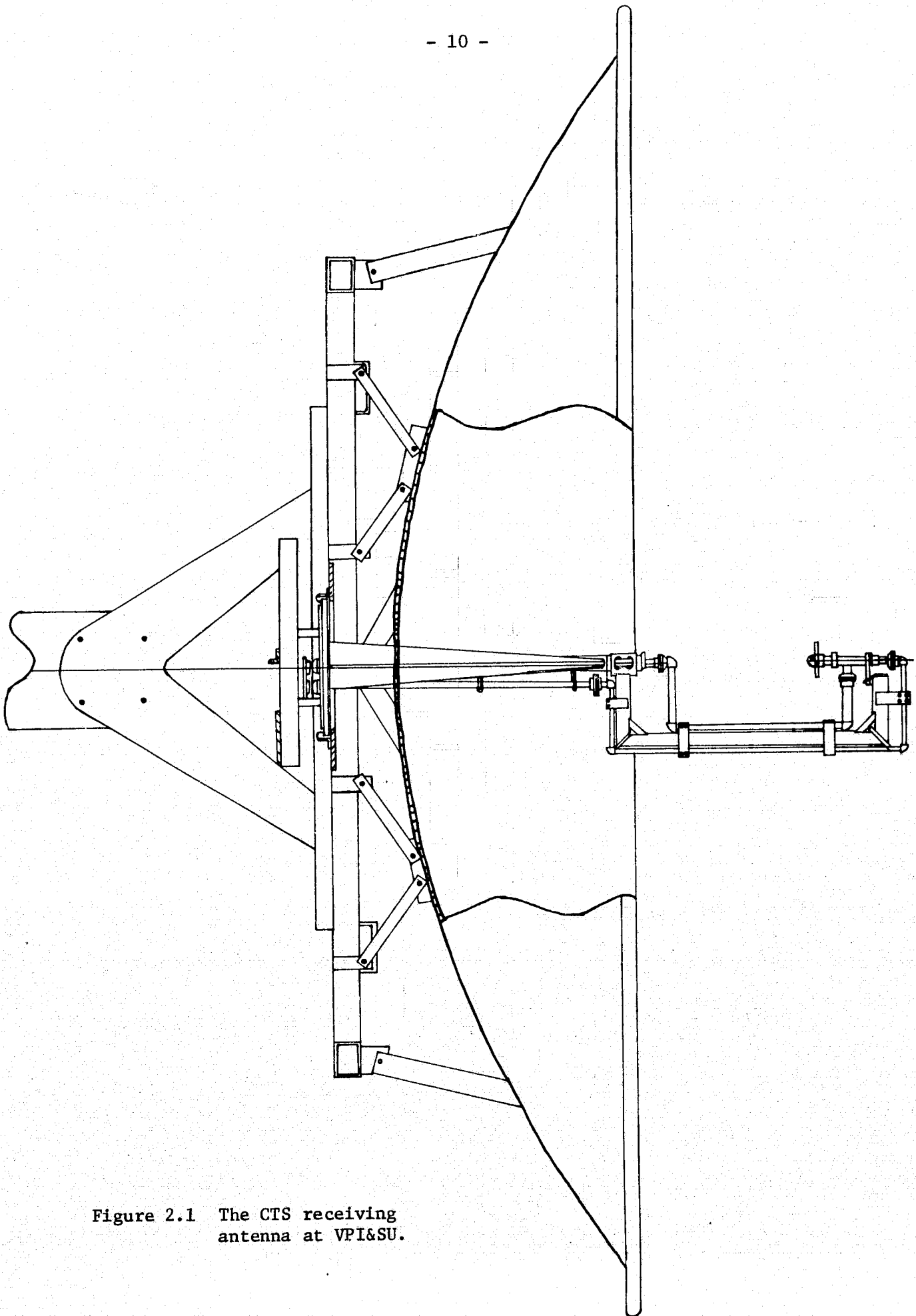


Figure 2.1 The CTS receiving antenna at VPI&SU.

Table 2.1. Antenna Specifications and Test Data

	<u>Specification</u>	<u>Test Data</u>
Frequency:	11.70 GHz primary 11.843-11.928 secondary (with perhaps some degradation of performance)	
Reflector size:	12 foot diameter parabola of revolution	
Reflector surface tolerance:	0.025 inch RMS or better	
Feed system:	prime focus with multimode feed horn	
Output polarizations:	Right hand circular and left hand circular in one configuration; and orthogonal linear polarizations in the other configurations. These two outputs states are manually selectable.	
Polarization position:	manually rotatable $\pm 90^\circ$	manually rotatable 360°
Port-to-port isolation:	30 dB minimum	45.7 dB at 11.700 GHz
f/D:	0.33	
Gain	50 dBi	50.85 dBi
Aperture efficiency:	greater than 60%	
Radiation pattern:	-20 dB or lower sidelobes 0.5° half power beam width	-30 dB for RHC
Crosspolarization level:	-18.5 dB (axial ratio of 2.0 dB) over main beam out to -10 dB; -35 dB (axial ratio 0.3 dB) on boresight	For RHCP: -35 dB (axial ratio 0.30 dB) on-axis and -19.2 dB (axial ratio 1.9 dB) at -10 dB pattern point. For LHCP: -36.2 dB (axial ratio 0.27 dB) on-axis and -18.8 dB (axial ratio 2.0 dB) at -10 dB pattern point.

	<u>Specification</u>	<u>Test Data</u>
Insertion losses:		
Waveguide from feed to base of reflector:	0.4 dB or less	
Polarizer:	0.1 dB or less	
OMT:	0.1 dB or less	
VSWR:	1.15	RHCP: 1.11 LHCP: 1.12
Antenna noise temperature:	20°K at 32° elevation angle	Comment: Clear air atmospheric noise is 10°K. Maximum ground pick-up plus atmospheric noise gives an antenna temperature of 36°K. Thus 20°K is assumed.
Total antenna weight:	500 lbs.	
Feed horn protection:	Mylar windor	
Support spars:	none	
Output waveguide:	WR 75	
Environmental specifications:		
Temperature:	-50°F to 130°F	
Wind loading:	Operates normally for winds below 40 mph. Must be stowed in a zenith pointing position for winds above 40 mph.	

of the wave, w , and the antenna, a , or $m_p = m_p(w, a)$.

Assume that the antenna is dual polarized with a co-polarized state a_c and cross-polarized state a_x . The available power outputs for each antenna state are then

$$W_c = m_p(w, a_c) S A_{ec} \quad (2)$$

and

$$W_x = m_p(w, a_x) S A_{ex} \quad (3)$$

The isolation (I) is the ratio of (2) to (3)

$$I = \frac{W_c}{W_x} = \frac{m_p(w, a_c) A_{ec}}{m_p(w, a_x) A_{ex}} \quad (4)$$

Usually the effective apertures for the co- and cross-polarized cases are the same; then (4) becomes

$$I = \frac{m_p(w, a_c)}{m_p(w, a_x)} \quad (5)$$

We now have an expression for the isolation as a function of the co- and cross-polarization states and the polarization state of the incoming wave.

For the co-polarized channel performance, the loss encountered due to polarization mismatch is given by

$$L_m = -10 \log m_p(w, a_c) \quad [\text{dB}] \quad (6)$$

With this background the clear weather poalrization response of our system can be calculated. Since we are working with nearly circular polarization the following formualtion for the polarization mismatch factor

is convenient

$$m_p(w, a) = \frac{1}{2} + \frac{4 AR_w AR_a + (AR_w^2 - 1)(AR_a^2 - 1) \cos 2 \Delta\tau}{2 (AR_w^2 + 1)(AR_a^2 + 1)} \quad (7)$$

where

AR_w = axial ratio of incoming wave*

AR_a = axial ratio of antenna*

$\Delta\tau$ = angular separation of major axes of wave and antenna polarization ellipses.

Given the dependence of (7) on $\Delta\tau$, it is obvious that rotation of the antenna feed, which changes $\Delta\tau$, affects m_p and thus the isolation.

It is instructive to examine (7) for a few special cases.

Example 1: Perfect RHCP wave and perfect RHCP antenna. Then $AR_w = -1$

and $AR_a = -1$ and

$$m_p = 1 \quad . \quad (8)$$

Example 2: Perfect RHCP wave and perfect LHCP antenna. Then $AR_w = -1$

and $AR_a = +1$ and

$$m_p = 0 \quad . \quad (9)$$

These two examples form a perfect dual polarization system. There is no mismatch loss since (8) in (6) yields $L_m = 0$ dB. Also (8) and (9) in (5) yield $I(\text{dB}) = +\infty$.

* In this report we will adopt the convention that a right-hand polarized wave has a negative axial ratio and a left-hand polarized wave has a positive axial ratio.

Example 3: Perfect RHCP wave and linearly polarized antenna. Then

$AR_w = -1$ and $|AR_a| = \infty$, and (7) yields

$$m_p = \frac{1}{2} \quad (10)$$

independent of $\Delta\tau$. This corresponds to a mismatch of

$$L_m = 3 \text{ dB} \quad (11)$$

Example 4: Wave and antenna with identical axial ratios. Let

$$AR_w = AR_a = AR \quad (12)$$

Then (7) reduces to

$$m_p = \frac{1}{2} + \frac{4 AR^2 + (AR^2 - 1)^2 \cos 2 \Delta\tau}{2 (AR^2 + 1)^2} \quad (13)$$

If the major axes are aligned, $\Delta\tau = 0^\circ$,

$$m_p = 1 \quad (14)$$

and the system is perfectly matched!

Example 5: Wave and antenna with identical axial ratio magnitudes but opposite sense. Let

$$AR_w = AR \quad \text{and} \quad AR_a = -AR \quad (15)$$

Then (8) reduces to

$$m_p = \frac{1}{2} + \frac{-4AR^2 + (AR^2 - 1)^2 \cos 2 \Delta\tau}{2 (AR^2 + 1)^2} \quad (16)$$

The closer AR is to unity the closer m_p approaches zero. Also notice that if $\Delta\tau = 90^\circ$

$$m_p = 0 \quad (\Delta\tau = 90^\circ) \quad (17)$$

independent of AR.

These examples illustrate the theoretical operation of our antenna system. Examples 1 and 2 are the ideal co- and cross-polarized responses. Example 3 predicts the ideal behavior when the feed horn is in the linear output position (it is, of course, normally in the circular position). Examples 4 and 5 demonstrate the behavior if the axial ratios of the antenna responses and the wave happened to be of the same magnitude. These last two examples also indicate that if the receiving antenna had an adjustable axial ratio in addition to adjustable tilt angle, the mismatch loss and isolation could be optimized as the incoming wave state changed.

2.3.2 Maximum and Minimum Isolation Values

If equation (5) is written in terms of the wave axial ratio AR_w , the co-polarized channel axial ratio AR_c , and the cross-polarized channel axial ratio AR_x , the result is a completely general expression for isolation under all conditions:

$$I = \frac{\frac{(AR_w^2 + 1)(AR_c^2 + 1) + 4 AR_w AR_c + (AR_w^2 - 1)(AR_c^2 - 1) \cos 2 \Delta\tau_c}{2(AR_w^2 + 1)(AR_c^2 + 1)}}{\frac{(AR_w^2 + 1)(AR_x^2 + 1) + 4 AR_w AR_x + (AR_w^2 - 1)(AR_x^2 - 1) \cos 2 \Delta\tau_x}{2(AR_w^2 + 1)(AR_x^2 + 1)}} \quad (18)$$

The quantities $\Delta\tau_c$ and $\Delta\tau_x$ measure the angles between the major axes of the incoming polarization ellipse and the polarization ellipses of the co-polarized and cross-polarized antenna feeds.

In most circularly polarized systems (as in the CTS situation) all axial ratios are nearly unity in magnitude. Under these conditions the co-polarized output varies only slightly as $\Delta\tau_c$ is changed. This can be seen by examining the numerator of (18) which is the polarization mismatch factor for the wave and the co-polarized receiving state. Since AR_w and AR_c are of the same sign and near unity in magnitude, the last term is negligible. Then (18) is approximately given by

$$I \approx \frac{(AR_w^2 + 1)(AR_c^2 + 1) + 4 AR_w AR_c}{(AR_w^2 + 1)(AR_x^2 + 1) + 4 AR_w AR_x + (AR_w^2 - 1)(AR_x^2 - 1) \cos 2 \Delta\tau_x} \cdot \frac{AR_x^2 + 1}{AR_c^2 + 1} \quad (19)$$

Maximum isolation occurs when the wave ellipse major axis is perpendicular to the cross-polarized antenna major axis, i.e. when $\Delta\tau = 90^\circ$. Then (19) gives

$$I_{\max} = I(\Delta\tau_x = 90^\circ) \approx \frac{(AR_w^2 + 1)(AR_c^2 + 1) + 4 AR_w AR_c}{2(AR_w + AR_x)^2} \frac{AR_x^2 + 1}{AR_c^2 + 1} \quad (20)$$

Minimum isolation occurs for $\Delta\tau_x = 0^\circ$, and (19) yields

$$I_{\min} = I(\Delta\tau_x = 0^\circ) \approx \frac{(AR_w^2 + 1)(AR_c^2 + 1) + 4 AR_w AR_c}{2(AR_w AR_x + 1)^2} \frac{AR_x^2 + 1}{AR_c^2 + 1} \quad (21)$$

In an operational situation the system isolation will fall somewhere between I_{\max} and I_{\min} . If the antenna feed were rotated (and proper alignment maintained) the isolation should vary smoothly between these extremes.

The VPI&SU antenna has these parameters on boresight

$$AR_c \text{ (dB)} = 0.3 \text{ dB}$$

$$AR_c = -1.03514 \text{ (RHCP)}$$

$$AR_x \text{ (dB)} = 0.27 \text{ dB}$$

$$AR_x = 1.03157 \text{ (LHCP)}$$

and from them we may calculate the expected maximum and minimum isolations as a function of the axial ratio of the satellite signal. The results are summarized in Table 2.2.

Table 2.2. Predicted Isolation Limits

$AR_w \text{ (dB)}$	AR_w	$I_{\max} \text{ (dB)}$	$I_{\min} \text{ (dB)}$
0	-1	36.2	36.2
0.3	-1.03514	58.3	29.7
0.5	-1.05925	37.6	27.1
0.7	-1.08393	32.1	25.1
1.0	-1.12202	27.5	22.7

2.4 Observed Antenna Performance

The feed rotation tests which have been conducted thus far are somewhat inconclusive due to slight changes in feed position with rotation. When

the axial ratios of the antenna and the incoming wave are nearly matched the observed isolation is extremely sensitive to small changes in AR_c and AR_x . These in turn vary with feed position and with the angle of incidence of the incoming wave with respect to the antenna boresight axes.

By very careful adjustment of the feed rotation angle and the antenna pointing coordinates it is possible to measure isolations of 45 dB. An isolation of this magnitude is unrealistic, though, as it cannot be maintained by the tracking system as the spacecraft moves. If the tracking program is adjusted for peak co-polarized response, the observed isolation ranges from about 30 to 35 dB in a 24-hour period. This range is representative of what could be expected in an operational dual polarized communications system and is more than adequate for this experiment.

3. The RF Front End

3.1 Description

Figure 3.1 is a block diagram of the VPI&SU CTS RF front end. Manufactured by LNR Communications, Inc. of Hauppauge, New York, it is a dual channel 11.7 GHz receiver with a common local oscillator (LO) that insures phase coherence. The RF front end is mounted on a rotatable feed assembly behind the antenna reflector.

Channel 1 designates the part of the receiver that processes the co-polarized received signal. The 11.7 GHz input signal at J_1 is downconverted to 1.05 GHz and amplified. The 1.05 GHz output is at J_2 . J_3 is the local oscillator input from the common LO located inside channel 2. J_4 is the bias voltage input which is also derived from channel 2, the section that processes the cross-polarized signal. E_1 is a chassis ground connected to the pedestal. Table 3.1 lists the specifications and actual performance of channel 1.

Table 3.1. Performance and specification data for channel 1

	<u>Specification</u>	<u>Measured</u>
Gain	37.0 dB	41.5 dB
Gain Stability	$\pm .3$ dB/24 HRS	0 dB/67 Hrs
Noise Temperature	1540° K	962° K
Input VSWR	1.4:1	1.35:1
Output VSWR	1.1:1	1.08:1
Spurious Output Level	-60 dB	None
1 dB Gain Compression Point	-70 dBm	-60 dBm

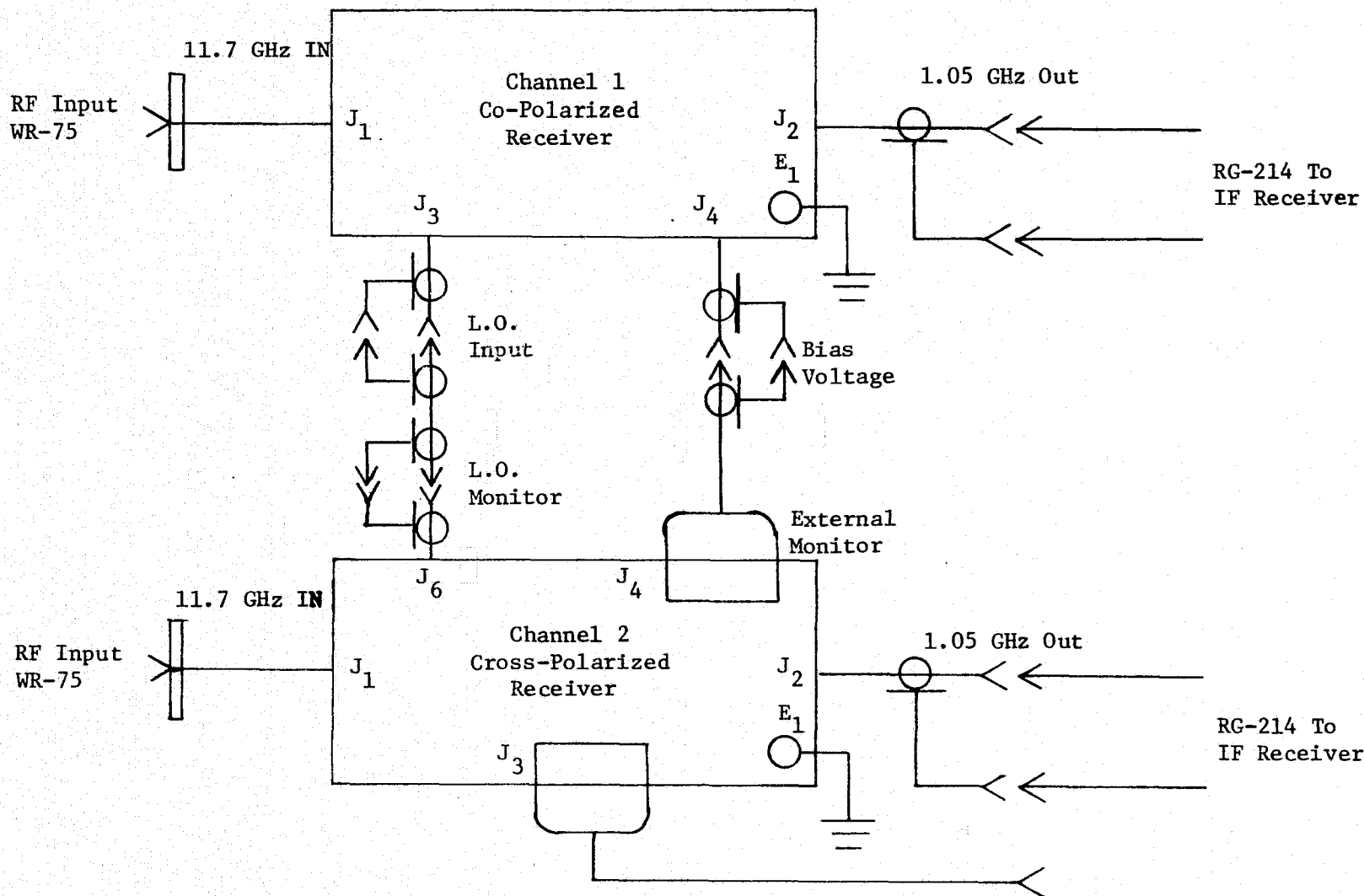


Figure 3.1. VPI&SU CTS Beacon RF Front End Block Diagram

In channel 2 the 11.7 GHz cross-polarized signal at J_1 is amplified by a non-cryogenic parametric amplifier and then down converted to 1.05 GHz. The signal is then amplified again before the IF output at J_2 . J_3 is the AC power source input and E_1 is a chassis ground connected to the pedestal. Table 3.2 lists the specifications and actual performance data for channel 2.

Table 2.2. Performance and specification data for channel 2

	<u>Specification</u>	<u>Measured</u>
Gain (RF to IF)	72.0 dB	79.0 dB
Gain Stability	$\pm .3$ dB/24 HRS	$\pm .3$ dB/65 HRS
Noise Temperature	200.0° K	184.4° K
Input VSWR	1.1:1	1.1:1
Output VSWR	1.15:1	1.12:1
Spurious Output Level	-60 dB	None
1 dB Gain Compression Point	-75 dBm	-69.0 dBm

3.2 Proposed Calibration System

At present all on-site calibration of the RF front end has been done using the CTS spacecraft as a calibration source. Assuming FCC licensing approval we intend to install a remote-controlled calibration system for periodic verification of RF front performance. It will be located on the roof of McBryde Hall, approximately 1600 meters east of the VPI&SU earth station.

Figure 3.2 is a block diagram of the calibration system. It is built around an 11.7 GHz crystal-controlled oscillator providing a 10 dBm output.

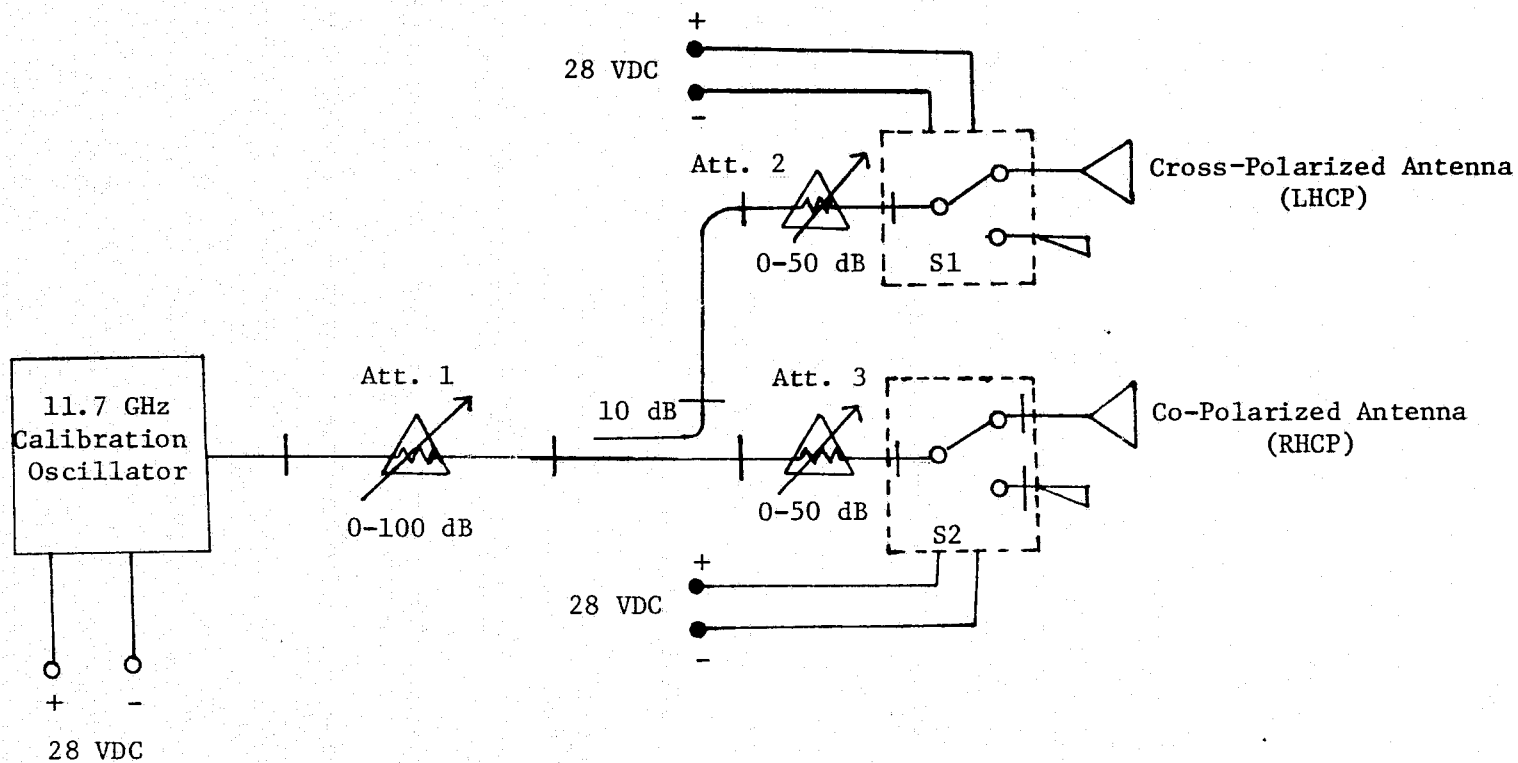


Figure 3.2. VPI&SU CTS Earth Terminal Calibration Transmitter

Based on the measured RF front end performance, Table 3.3 illustrates the calculation of the power levels that the system must deliver to its transmitting antennas.

Table 3.3. Calibration system power budget

	<u>Co-polarized Channel</u>	<u>Cross-polarized Channel</u>
Saturation Input to IF Receiver	-77.5 dBm	-50.0 dBm
Coaxial Cable Loss (To RF Front End)	6 dB	6 dB
RF Front End Gain	41.5 dB	79.0 dB
Antenna Gain (Receive)	50.8 dB	50.8 dB
Spreading Loss	117.5 dB	117.5 dB
Antenna Gain (Transmit)	<u>17.5 dB</u>	<u>17.5 dB</u>
Power Required at Transmit Antenna	-63.8 dBm	-73.8 dBm

Since the two required power levels are 10 dB apart, a 10 dB coupler is appropriate for the power divider. With Attenuator 2 and Attenuator 3 set to 0.0 dB, Attenuator 1 is set to 73.8 dB. This allows Attenuator 2 and Attenuator 3 to calibrate the IF receivers over a 50 dB dynamic range. The co-polarized antenna will be RHCP and the cross polarized antenna will be LHCP. The two channels may be terminated independently of one another by a matched load through S1 and S2 whenever the calibrator is not used.

This type of calibration system provides a means for checking the gain and linearity of the RF front end under operational conditions. At first glance it would seem possible to check linearity with the satellite signal

by inserting a precision attenuator between the main receiving antenna and the RF front end, but the thermal noise added by the attenuator makes this procedure unworkable.

4. The IF Receiving System

4.1 System Description

The IF signal processor for the CTS project was constructed using two Martin Marietta ATS-5 IF receivers as the starting point. Many improvements were made to the original design which greatly increased the overall sensitivity and dynamic range. These modifications are described in detail in the next section. Refer to Figure 4.1 for the following description of the CTS IF signal processor.

The co-polarized channel signal input is coupled to the receiver through a 9 dB attenuator to achieve the proper dynamic range. The signal is down-converted to 60 MHz where it passes through two wide-band amplifiers and through a 6 dB attenuator to a 60 MHz crystal filter. The attenuator adjusts the dynamic range. The crystal filter greatly reduces the bandwidth and therefore the noise so that the noise does not overdrive the following stages. The signal is amplified further at 60 MHz and then down-converted to 10 MHz. The 10 MHz signal passes through a low pass filter and another 6 dB attenuator (for dynamic range control) before being amplified by the 10 MHz variable gain amplifier. Up to this point the receiver configuration is basically the same as the Martin-Marietta ATS-5 receiver. The cross-polarized signal channel is also very similar up to this point, although the attenuators and the lack of one wide band amplifier produce a different dynamic range.

Phase locking of the received signals is done at 10 MHz by the co-polarized channel because this signal is usually stronger than the cross-polarized signal. The power divider delivers half of the power of the

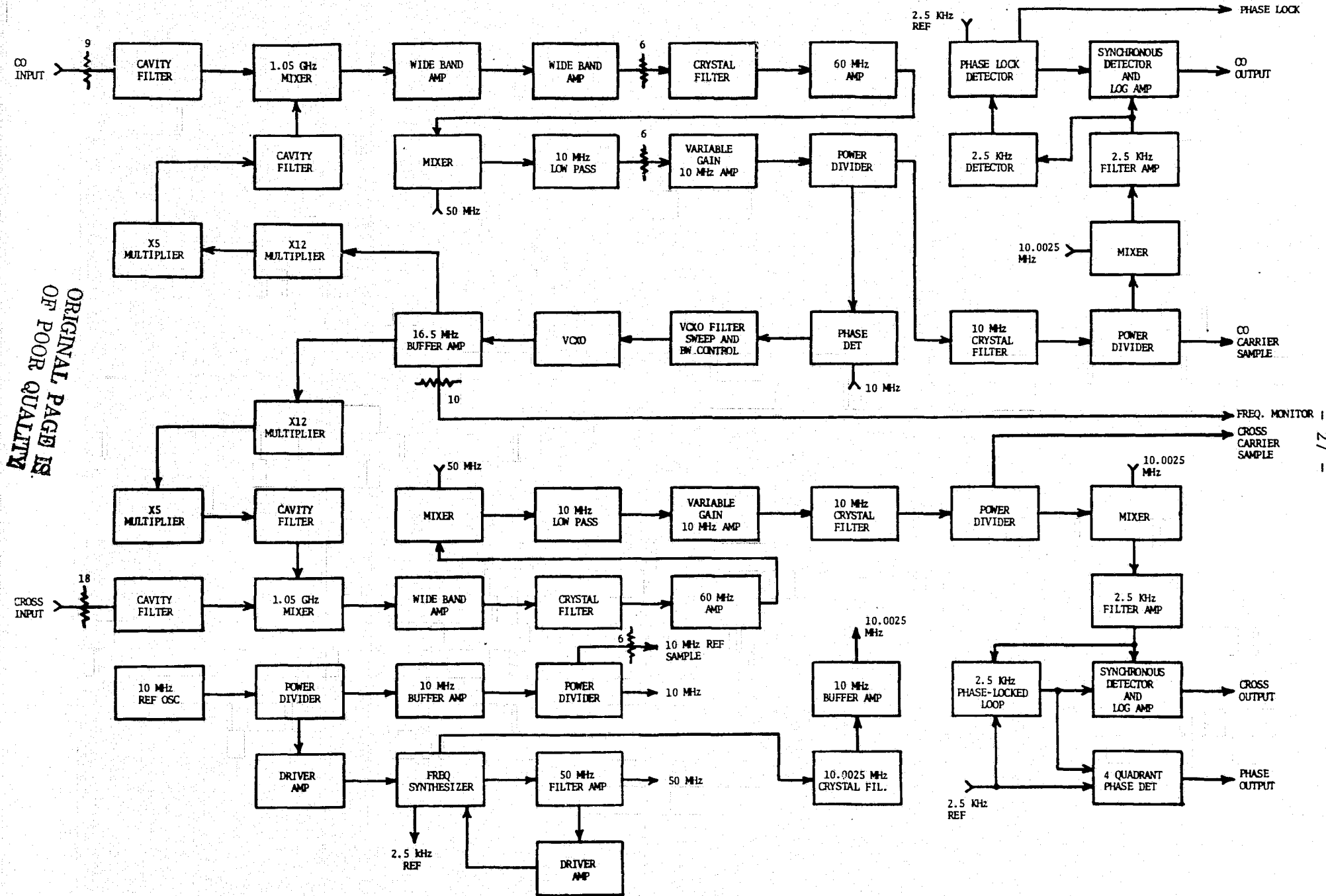


Figure 4.1. Block diagram of the IF receiving system.

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10 MHz co-polarized signal to the phase detector where it is compared to the 10 MHz reference oscillator. The error signal from the phase detector passes to the VCXO filter, sweep, and bandwidth control circuit. This circuit was designed at VPI&SU and is described in detail in the next section. Its use has increased the locking sensitivity of the receiver by about 20 dB. The control signal developed by this circuit is applied to the voltage controlled crystal oscillator (VCXO) which has a nominal frequency of 16.5 MHz. The oscillator signal is amplified by the 16.5 MHz buffer amplifier (also developed at VPI&SU) in order to increase the power level sufficiently to drive both receiver channels. A third output provides for frequency monitoring at the front panel. The 16.5 MHz oscillator output is multiplied by 60 (X12 followed by X5) to produce the 990 MHz local oscillator signal for both channels. Hence the cross-polarized channel is always tuned to exactly the same frequency as the co-polarized channel, and no phase locking at 10 MHz is needed in the cross-polarized channel.

The second output of the power divider goes through a 10 MHz crystal filter and another power divider to a mixer. Here the signal is down converted to 2.5 KHz. This circuitry is identical for both channels. The co-polarized signal goes through a 2.5 KHz filter-amplifier to the synchronous detector and logarithmic amplifier to produce the co-polarized output level. The synchronous detector and logarithmic amplifier unit, developed at VPI&SU, greatly improved the sensitivity and dynamic range of the original Martin Marietta receiver and it is described in detail in the next section. It receives a reference signal from the phase lock detector circuit; the presence of the reference also indicates when the co-polarized signal is phase locked to the 10 MHz reference oscillator. The 2.5 KHz detector shown

in Figure 4.1 is the original detector designed by Martin-Marietta. It is needed only to drive the phase lock detector.

After down conversion to 2.5 KHz the cross polarized signal is routed through a 2.5 KHz filter amplifier and into a synchronous detector and logarithmic amplifier to produce the cross-polarized output level. However, since the cross-polarized signal is not phase locked to the 10 MHz reference oscillator there is no reference signal available for the synchronous detector. The 2.5 KHz phase locked loop was designed and built to overcome this difficulty. Its operation is described in detail later. Essentially it shifts the phase of the 2.5 KHz reference (which is phase locked to the co-polarized signal) so that it is in phase with the cross-polarized signal. The synchronous detector requires this in-phase condition. A convenient method for measuring phase between the co and cross signals resulted from this scheme.

The input and output signals of the 2.5 KHz phase locked loop represent the phases of the co-polarized and cross-polarized signals respectively. These are applied to a four-quadrant phase detector (developed at VPI&SU and described later) which indicates the relative phase difference between the co-polarized and cross-polarized signals.

4.2 Modifications to the ATS-5 Receivers

4.2.1 Introduction

The circuits described in this section were designed and built at VPI&SU and have greatly improved the performance of the ATS-5 IF signal processors. All are currently being used on the CTS project.

4.2.2 VCXO Filter, Sweep and Bandwidth Control Circuit

The VCXO filter, sweep and bandwidth circuit is essentially the same circuit used in the ATS-6 experiment. It is a new design which replaced the original circuit in the ATS-5 IF receiver. The circuit was designed by P. H. Wiley. The difficulties encountered with the original circuit and the details of resolving those difficulties are described explicitly in the Final Report, A 20 GHz Depolarization Experiment Using the ATS-6 Satellite, Contract NAS5-21984, September 10, 1975.

Briefly three major problems were inherent in the original ATS-5 VCXO sweep circuit: (1) gross unbalance in the error signal integrator which would cause the sweep to be speeded up, slowed down, stopped, or reversed during the sweep operation. During lock, the unbalance would cause the circuit to be pulled out of lock; (2) the ramp-generating integrator capacitor discharged during lock which tended to cause the VCXO control voltage to decrease. The circuit would have to pull out of lock slightly in order for the error signal integrator to correct for the decrease in ramp voltage; (3) the circuit produced only a ± 2.5 volts maximum output, and the VCXO required a ± 5 volts signal to cover its full frequency range.

The problems were resolved by the design and installation of a new VCXO filter, sweep and bandwidth control circuit shown in Figure 4.2. Operational amplifier A1 performs both functions of sweep and phase lock. It must be selected to have a smaller non-inverting offset current than inverting so that the offset current can be compensated by the potentiometer on pin 3. MOSFET Q1 allows sweep to occur when it is turned on and stops the sweep when it is turned off. The sweep stop signal is produced by the phase lock detection circuit. The filter characteristics of A1 are the same as

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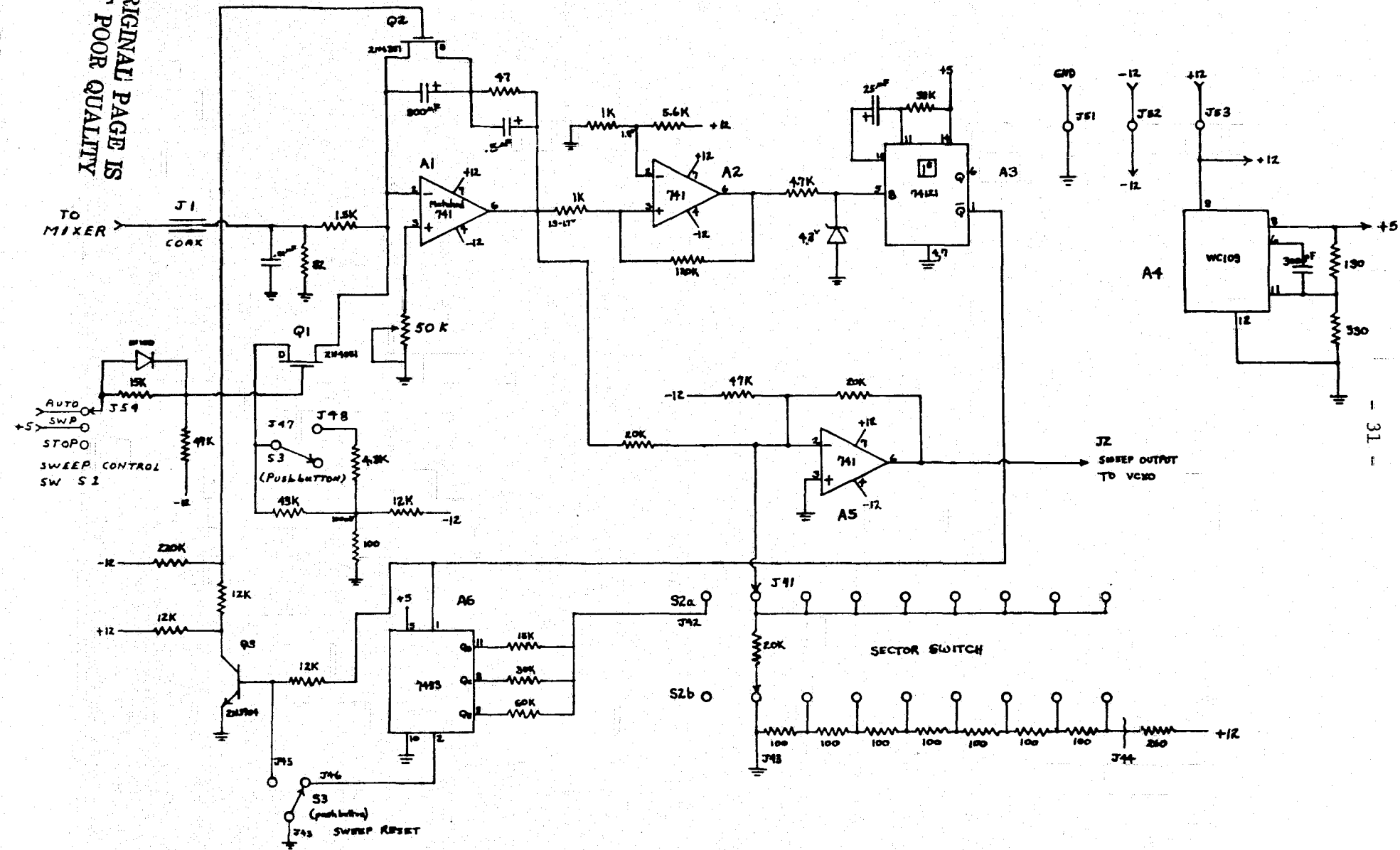


Figure 4.2. VCXO filter, sweep, and bandwidth control circuit.

those of the original circuit. The capacitors have been increased by a factor of 80 and the resistors decreased by the same factor. This alone increases the stability by 80 times as explained in the ATS-6 Final Report. Operational amplifier A2 serves as a comparator to detect the end of the desired sweep cycle. Device A3 is a one-shot multivibrator which generates a reset pulse at the end of each sweep cycle. Device A6 is used as a 3 bit binary counter to determine one of eight sectors in the automatic mode. The count in A6 is advanced by each reset pulse so that all eight sectors are swept sequentially. In the manual mode, sector switch S2 determines the sector to be swept. Op amp A5 sums the sector voltage to the control and sweep voltages for A1 and produces the output to the VCXO. Regulator A4 produces +5 volts for the logic.

The circuit was optimized for the 0.4 KHz/sec. sweep speed since this speed provides the greatest sensitivity and is in normal receiver operation used. A 3 position sweep control switch, S1, controls the sweep mode. In AUTO position the sweep stop signal from the phase detector controls the sweep. In SWP (sweep) position, +5 V DC is applied and the circuit is forced to sweep. In STOP position the open circuit stops the sweep. The sweep circuit has excellent stability and the VCXO will maintain its frequency for long periods of time. This mode is very useful in that it provides quick lock recovery in the instances where signal is removed temporarily for test purposes.

In the AUTO and SWP mode a 4 KHz/sec. speed can be acquired by manually closing pushbutton S3.

With the original ATS-5 circuit (and with everything adjusted as well as possible) the lower limit of signal into the IF receiver at 1.05 GHz

at which lock could be maintained was -118 dBm. The new circuit locks down to -134 dBm. In addition the circuit will sweep up to and lock onto a signal of -134 dBm. Previously the signal had to be at least -100 dBm to acquire lock. The potentiometers connected to pin 3 of A1 in Figure 4.2 were adjusted when the circuit was installed and have not required readjustment.

4.2.3 Buffer Amplifier

Slaving both IF receivers to the same VCXO requires that the VCXO drive two X12 multipliers. Also, the VCXO frequency is monitored by a counter. The oscillator output is not sufficient to drive these three units without buffering.

Figure 4.3 shows the circuit diagram of the 16.5 MHz buffer amplifier. One such amplifier is used to drive each of the X12 multipliers, and one drives the counter. The three amplifier inputs are connected in parallel. The amplifier gain is slightly greater than unity. The transistor operates at $I_C = 18$ mA, $V_{CE} = 8$ V. The transformer was wound with 7 turns and 2.5 turns of #22 wire on a small toroid. The transistor has $h_{fe} \approx 80$, $V_{CEO} \approx 30$ V, and $f_T \approx 300$ MHz.

4.2.4 Synchronous Detector

Improvements of the phase lock circuit in the ATS-6 IF receiver (installation of a new filter, sweep and bandwidth circuit) resulted in a capability to hold lock at a signal level far below that which the original detector could accurately measure. Therefore a new detector was incorporated in the IF receiver.

The technique used in this circuit is shown in Figure 4.4. The reference oscillator, which is phase locked with the input signal, is used to operate a synchronous switch. The input signal and associated noise are gated through

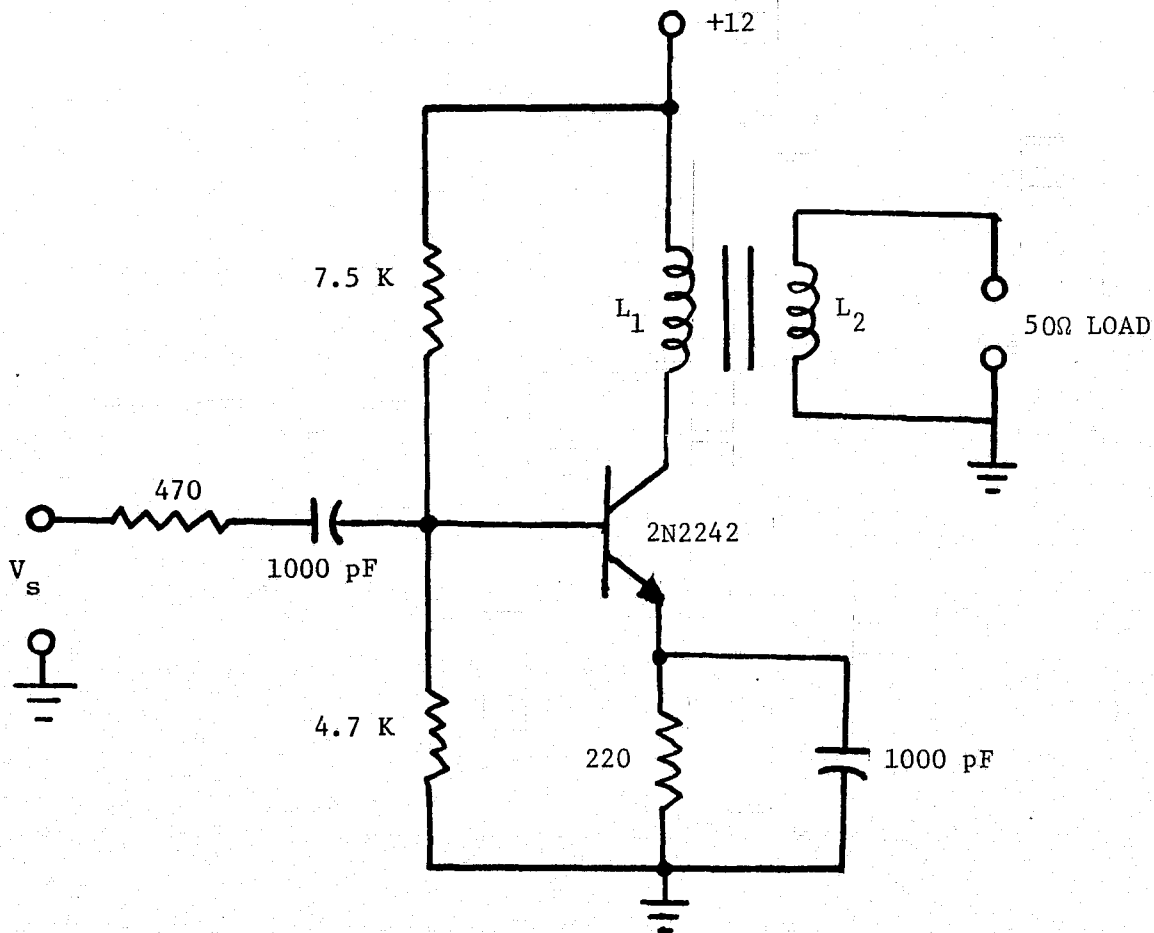


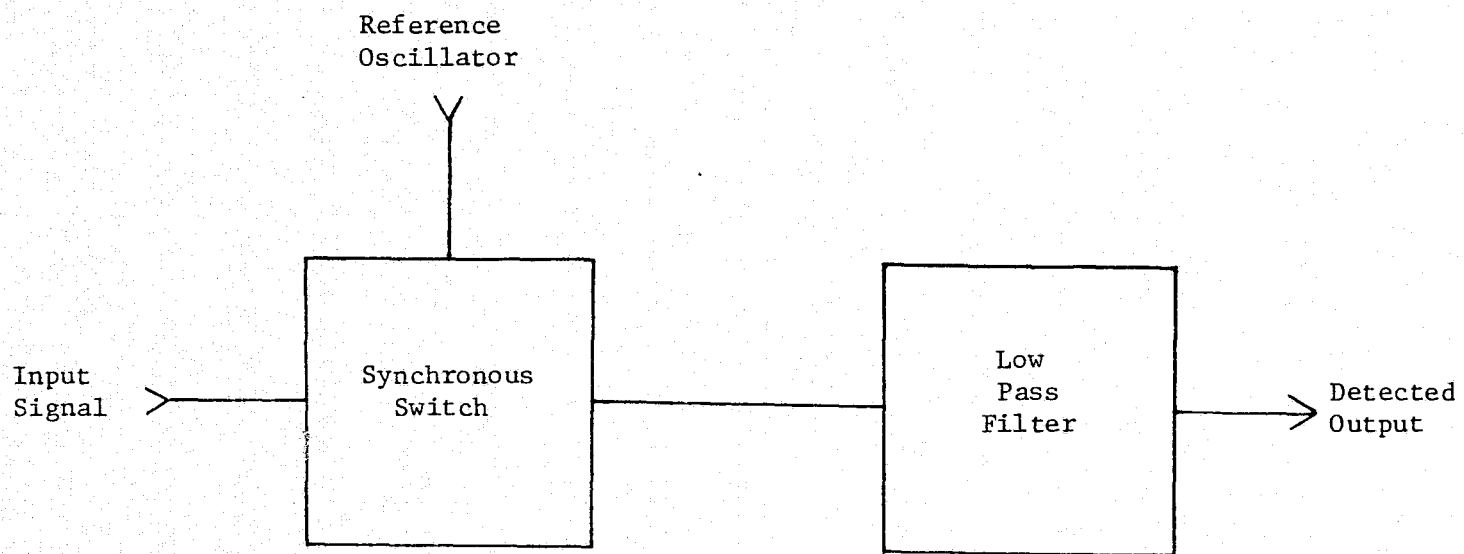
Figure 4.3. 16.5 MHz Buffer Amplifier

$$L_1 = 5 \mu\text{H}, L_2 = 0.6 \mu\text{H}, k = 0.97$$

the switch to the low pass filter during only a portion of the reference oscillator cycle. As a result of the action of the switch, only signals which are phase related to the reference oscillator produce a non-zero average value at the input to the low pass filter. Noise and signals which are not phase related to the reference oscillator produce an average value of zero. The time constant of the low pass filter is chosen to give the desired bandwidth. The output of the lowpass filter is a DC voltage representing carrier level whose variations are in accordance with the carrier modulation.

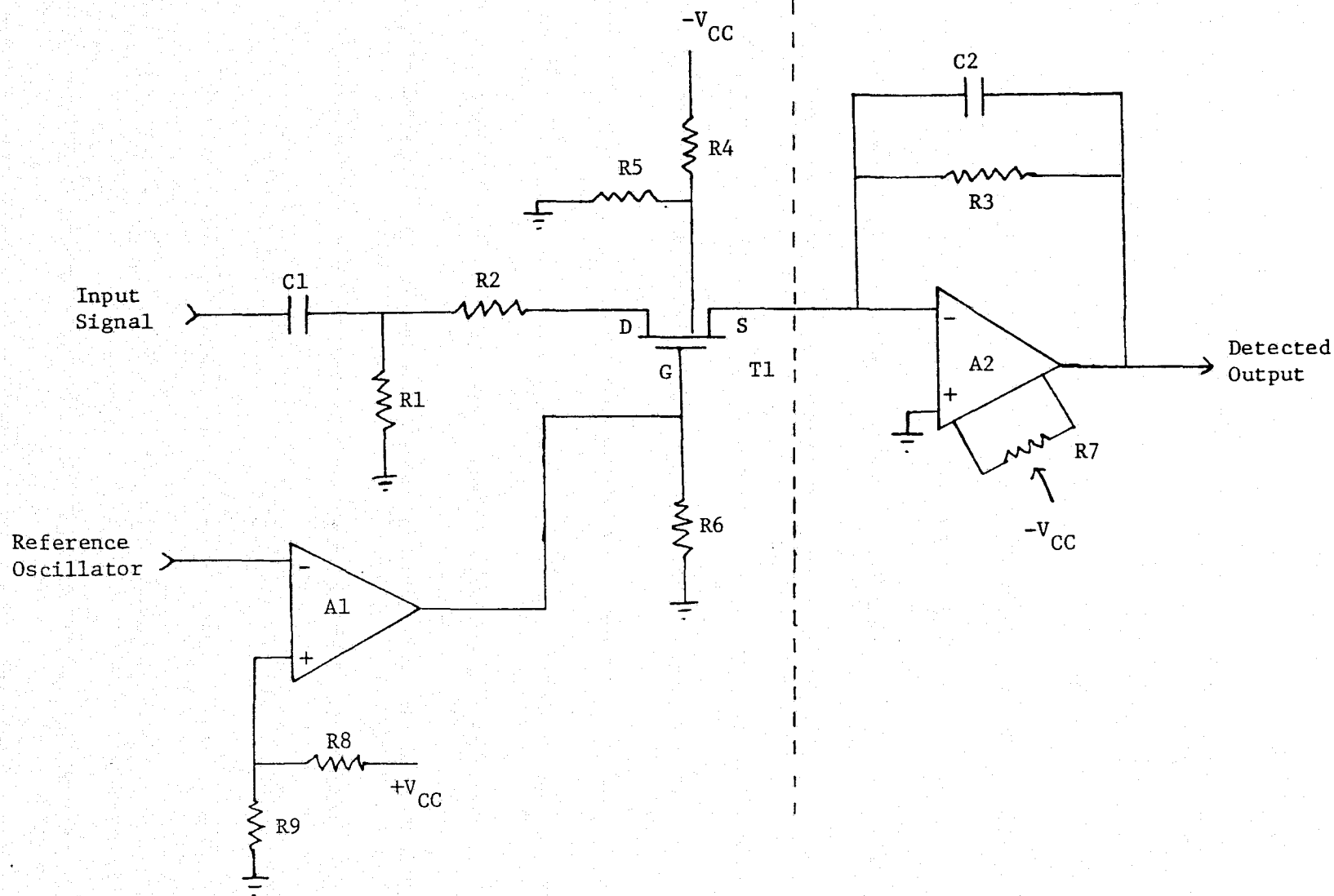
Figure 4.5 shows the circuit diagram of the practical realization of the detector. To facilitate a description of operation the circuit is divided functionally into the synchronous switch and the low pass filter. Capacitor C1 and resistor R1 form a DC blocking network to remove any DC component from the input signal. A DC component associated with the input signal would produce an undesired output. The input signal then passes through R2. The resistance of R2 fixes the gain of the entire circuit and hence the voltage output for a given input signal. The signal then passes to MOSFET transistor T1 which functions as a switch. When T1 is turned on the signal passes to the low pass filter. When it is off no signal is passed. Resistors R4, R5, and R6 serve only to bias T1 so that it will function as a switch. Operational amplifier A1 operates as an inverter and level shifter. The reference oscillator signal is a square wave with a minimum value of zero volts and a maximum value of +3 volts. Transistor T1 requires a voltage of +10 volts to turn it on and -10 volts to turn it off. When the reference oscillator is at zero volts the output of A1 is +10 volts. When the reference oscillator is +3 volts the output of A1 is

Figure 4.4. Block Diagram of Synchronous Detector



Synchronous Switch

Low Pass Filter



-10 volts. Resistors R8 and R9 bias A1 and determine the reference oscillator signal level at which the output of A1 changes from +10 volts to -10 volts.

The portion of the input signal which is passed by transistor switch T1 is coupled to the low pass filter. Operational amplifier A2 is operated as an integrator. The product of R3 in ohms and C2 in farads determines the time constant of the integrator. The reciprocal of the time constant is the bandwidth of the low pass filter in radians per second. Potentiometer R7 is an offset adjustment for A2 and is adjusted for zero volts out of A2 with only noise present at the input to the synchronous switch.

The complete synchronous detector circuit is shown in Figure 4.6 with final component values. The circuit is adjusted initially by applying only the clock signal and adjusting R1 for zero volts at point A.

The minimum signal level which could be measured before installation of the new detector in the ATS-6 receiver was about -110 dBm at the receiver input with a 5 dB post-detection signal to noise ratio (SNR). After installation of the detector the post-detection SNR was increased to 35 dB at an input signal level of -110 dBm. In addition the minimum signal level which could be measured with the new detector was -140 dBm and this resulted in a 5 dB signal to noise ratio at the detector output.

4.2.5 Logarithmic Amplifier with Extended Dynamic Range

Because the synchronous detector described in Section 4.2.4 provided a much wider signal level range, a new circuit to process the signal was necessary. A logarithmic amplifier with a single-polarity output voltage was needed, but it had to have a greater dynamic range than conventional

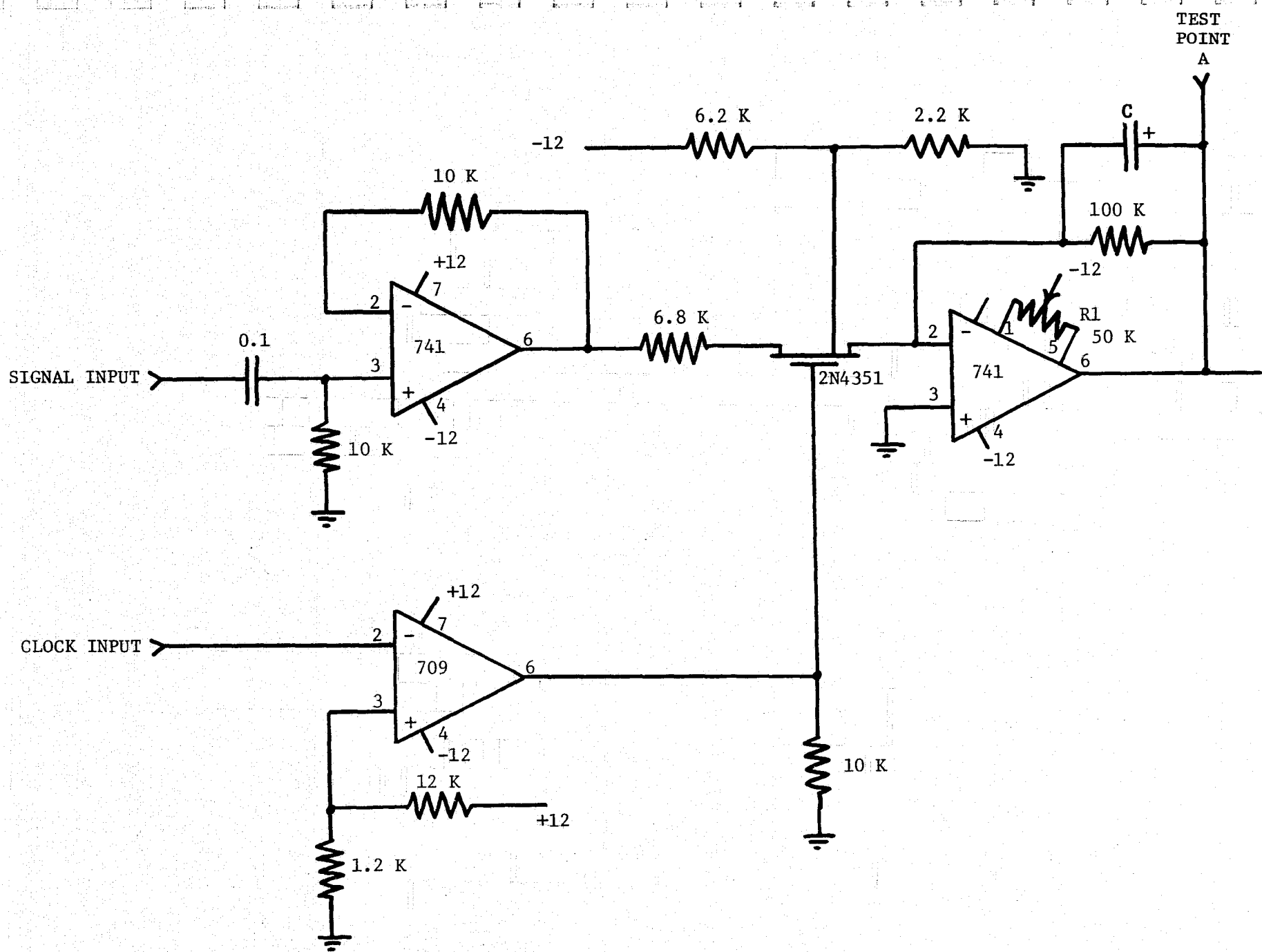


Figure 4.6. Final diagram of the synchronous detector.

log-amps used in a single-polarity mode.

The conventional log amplifier shown in Figure 4.7 has output voltage, V_o , given by

$$V_o = - \frac{kT}{q} \left[\ln \left(\frac{V_s}{R_1} + I_o \right) - \ln I_o \right] \quad (1)$$

k = Boltzmann's constant

T = temperature, °K

q = 1.6×10^{-19} C

I_o = diode D1 reverse saturation current

The input voltage V_s is supplied by a transducer which is external to the amplifier. The output voltage is not a reasonably accurate logarithmic function of the input voltage unless V_s/R_1 is several times greater than I_o . Therefore the lower limit on V_s is restricted to say 20 to 30 millivolts, or R_1 must be made unusually low which would load the transducer. In applications where transducer current is limited this conventional amplifier is not useful for input signal voltages less than about 20 millivolts.

The technique used in the CTS IF receivers is shown in Figure 4.8. The circuit incorporates a controlled current source where the current produced by the source is a constant times the input voltage, V_s . The output voltage, V_o , is given by,

$$-V_o = A \frac{kT}{q} \left[\ln(C V_s + I_o) - \ln I_o \right] \quad (2)$$

A = gain of amplifier A2

The constant C can be adjusted without altering the input impedance of amplifier A1. Therefore the circuit of Figure 4.8 can produce an output

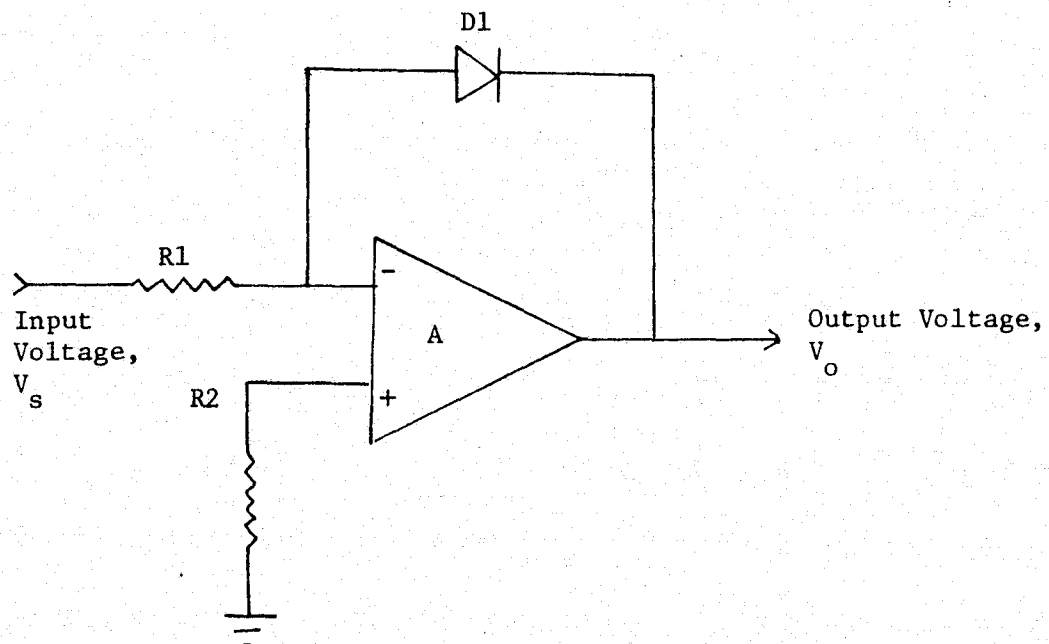


Figure 4.7. A conventional logarithmic amplifier.

voltage that is a reasonably accurate logarithmic function of input voltage for an arbitrarily small input voltage. The acceptable lower limit on input voltage is fixed only by the properties of amplifier A1, such as offset voltage and noise level.

The dynamic range of input voltage, V_s , can be selected to fit any given application simply by choosing the control constant, C , so that diode D1 operates in the exponential portion of its volt-ampere characteristic and always above the saturation current, I_0 . Obviously, amplifier A1 will have to be designed to process the range of input voltage selected. However, amplifier A1 does not have to exhibit logarithmic gain properties. Amplifier A1 has a unique control circuit which causes its output to be a very close approximation to input signal, V_s . Therefore amplifier A1 can be designed to accommodate signal levels ranging from microvolts to several volts.

The input impedance of amplifier A1 can be adjusted arbitrarily without degrading the logarithmic property of the circuit. For instances, amplifier A1 can be made to present a high input impedance, say 100 K ohms, regardless of dynamic signal range desired.

Amplifier A2 is used to buffer the diode signal and to provide a logic level signal range at the output.

A practical realization of the circuit is shown in Figure 4.9. A signal voltage, V_s , raises the noninverting node of A1 to almost V_s , depending on the values of $R1$ and $R2$. The output voltage of A1 tends to rise, which establishes a current in $R3$. A differential amplifier, A3, senses the voltage across $R3$ and the output voltage of A3 raises the inverting node of A1 to almost V_s . Therefore the output voltage of A1 becomes fixed such that voltage V_s exists across $R3$. A current exists in $R3$ equal to $V_s/R3$. This

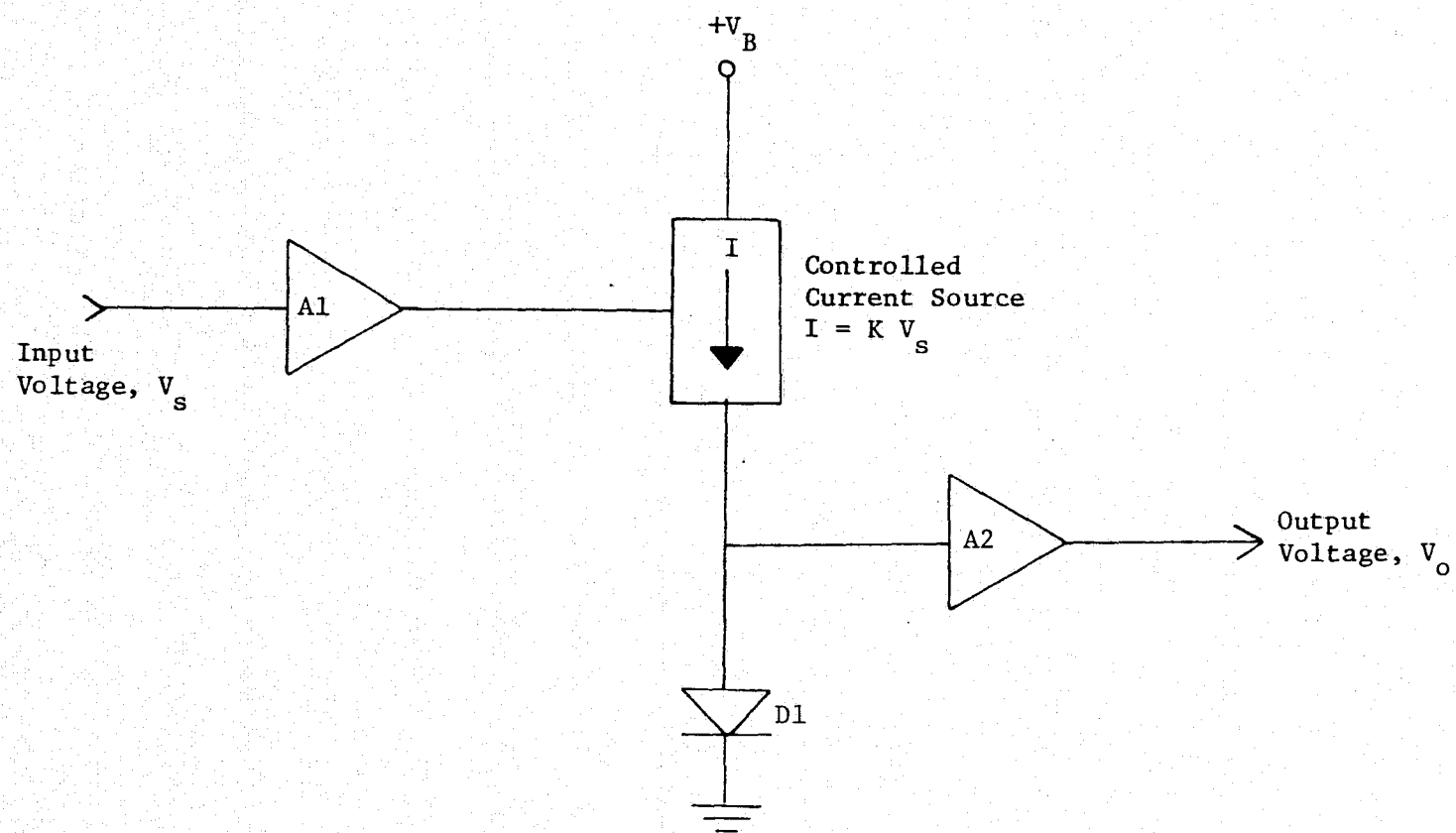


Figure 4.8. Basic circuit of the logarithmic amplifier.

controlled current flows through D1 establishing a voltage across D1 proportional to the logarithm of V_s .

The accuracy with which the current in R3 is $V_s/R3$ is set by the loop gain of A3 and A1. The loop gain can be large, consistent with the stability of the feedback circuit. The accuracy of the controlled current source is excellent, and of course, the circuit can be calibrated.

Resistor R3, amplifier A3, and the inverting gain of A1 constitute a voltage-controlled current source. Resistors R5, R6, R7, R8 fix the gain of A3. Resistors R1, R2, R4, R9 fix the gain of A1. Resistors R14, R15 and R16, R17 fix the noninverting and inverting gains of A2.

Diodes D1 and D2 are matched elements and placed side by side on the circuit board. Resistors R11, R12, R13 and V_{cc} and V_{ee} are used to bias D2 on with the anode at zero volts. If the temperature of D1 rises so will that of D2. The voltage change of D2 supplies an inverting signal to A2 which nullifies the signal from D1 produced by the temperature change. Diode D3 is included to prevent possible latch-up of A1. Capacitor C1 is used to provide additional high-frequency stability.

Note that by selecting R3 the current driving D1 can be set to a desired value for any V_s , provided amplifier A1 can produce the current. Therefore upon selection of the lower limit on V_s , the logarithmic element D1 can be set to "cut-on" level and V_s can be logarithmically amplified more accurately over a greater dynamic range than previously possible.

The lowest voltage V_s which the circuit can process is limited only by the noise of amplifier A1 and by the existence of DC input offset voltage at amplifier A1.

Note that the input impedance of A1 can be selected without altering the

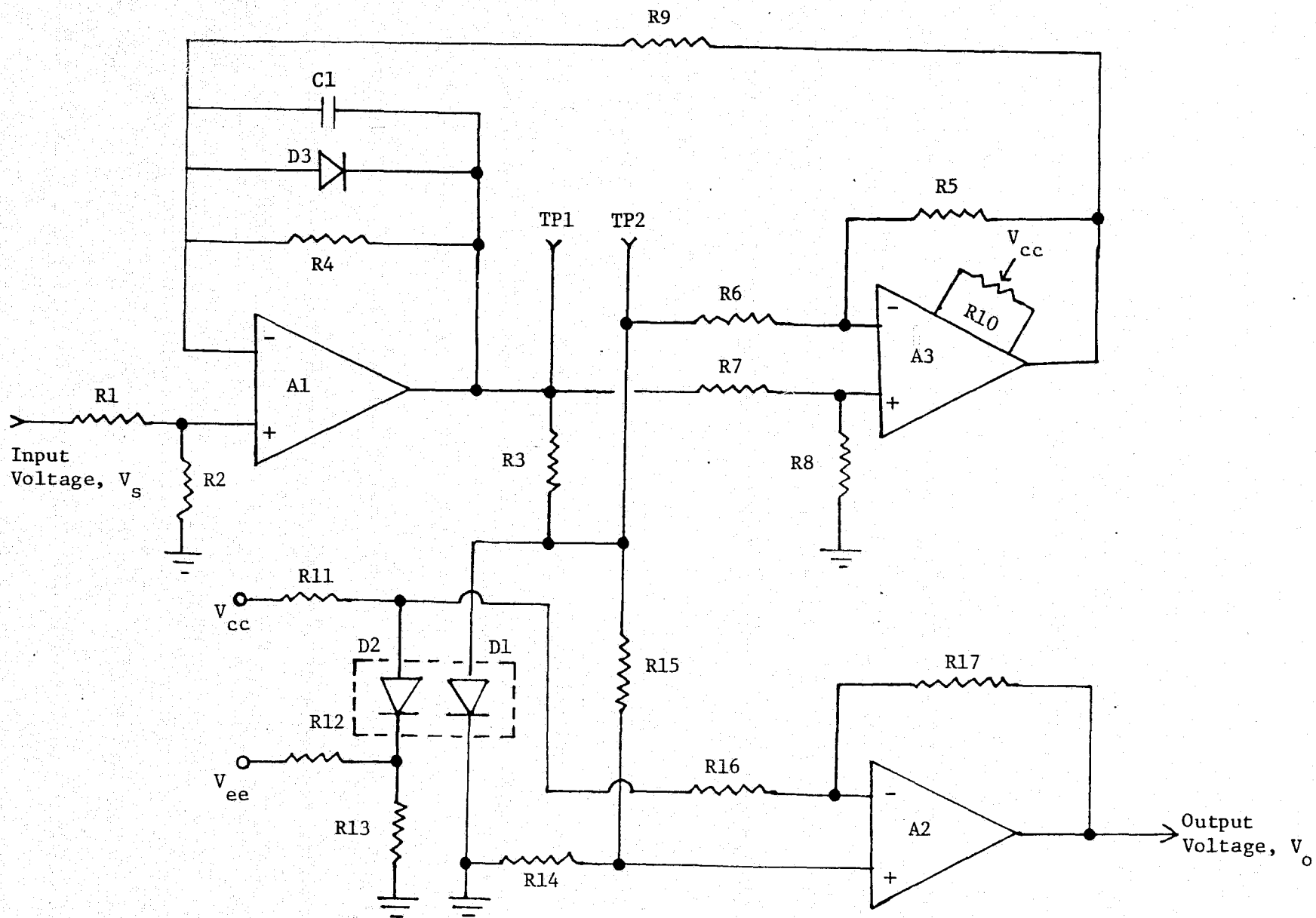


Figure 4.9. Complete logarithmic amplifier circuit.

circuit operation by selecting R1 and R2.

Potentiometer R10 is used to adjust the DC offset voltage of A3 such that the DC input offset of A1 is near zero volts.

Figure 4.10 shows the log-amp circuit with device identifications and component values. The circuit is adjusted initially by removing the signal, shorting TPD to TPC, and adjusting R2 for zero volts at TPB. The current source was adjusted for a current of 1.0 microamp per millivolt of signal. The lower limit on V_s was set at 1.0 millivolt. The output of A2 was designed to be a maximum of 10.0 volts when V_s was 10.0 volt. The input impedance of A1 was set at 100 K ohms. The circuit gave a very accurate logarithmic output for V_s of 1.0 millivolt to 10.0 volt. Thus the circuit has a dynamic range of 80 dB.

4.2.6 2.5 KHz Phase Lock Loop

The CTS IF Signal Processor is phase locked at 10 MHz on the co-polarized signal (only) because the co-polarized signal level is higher than the cross-polarized signal level. The co-polarized channel VCXO frequency is used as the mixer frequency (through the X60 multiplier) in the cross-polarized channel. The co receiver 10 MHz reference source also is used in the cross receiver. Without additional circuitry the advantage of the synchronous detector is lost in the cross-polarized receiver because the signal phase is random with respect to the 2.5 KHz reference square wave from the frequency synthesizer in the co receiver. Therefore a phase lock loop was designed for use in the cross receiver to bring the reference square wave into phase with the cross-polarized signal.

The primary objective of the circuit is to create an in-phase relation of the cross signal and the 2.5 KHz reference. However, a very simple and

accurate method of determining the phase between the co-polarized and cross-polarized signals resulted from the circuit design.

The phase-lock loop circuit is shown in Figure 4.11. The counter module is detailed in Figure 4.12. The signal frequency is fixed at 2.5 KHz by the locking action of the co receiver. As stated previously, the function of the circuit is to bring the 2.5 KHz reference into phase with the signal. Control of the phase lock loop is accomplished by the use of counters. A 1000-bit counter (slave) operates at a 2.5 MHz rate. An up-down counter (master) operates at selectable one-half multiples of 2.5 KHz, down to a 3.9 Hz rate; the rate is selected in a trade off between overshoot and jitter one one hand and the desired lock rate in degrees per second on the other. Counter storages are compared and when equal the circuit is reset and the cycle is repeated on the next trailing edge of the reference square wave. The signal and reference square wave are applied to a synchronous detector. These are 90° out of phase if the circuit is in lock; this makes the detector output zero and the master counter does not change count. Then the slave counter runs up to the same count and a constant delay results.

When the counts are matched, the output of the counter module then goes high and triggers a circuit which generates a 2.5 KHz square wave. Also, this circuit shifts the phase of the square wave by 90° so that it is in phase with the signal waveform. The reference square wave and signal are fed to the final output synchronous detector.

If the PLL synchronous detector output is not zero, the master counter will be moved during a cycle (2.5 KHz) and the slave counter will take a longer or shorter period of time to match it. The delay in opening the gate of the PLL synchronous detector will change until the detector output

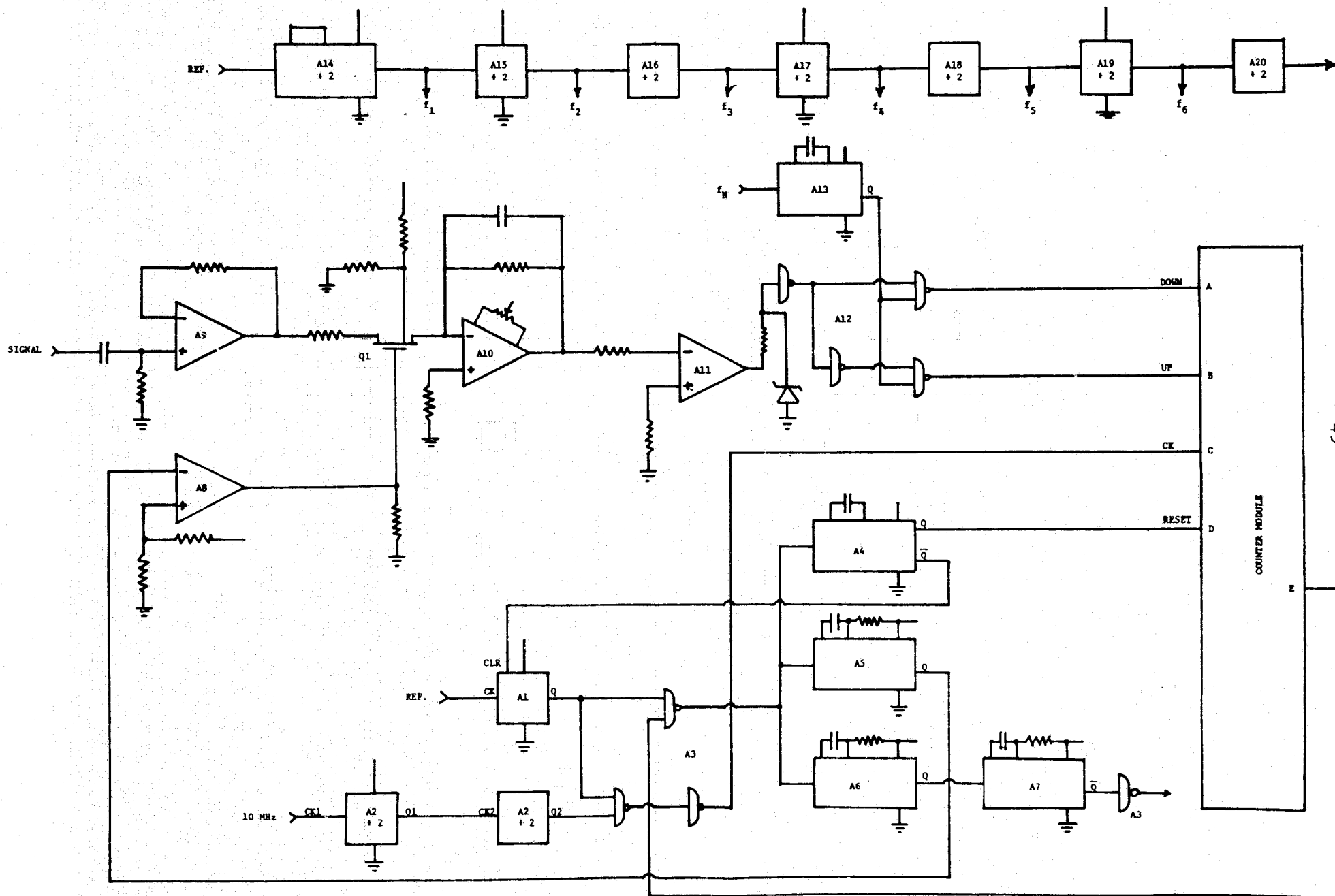


Figure 4.11. The phase locked loop circuit.

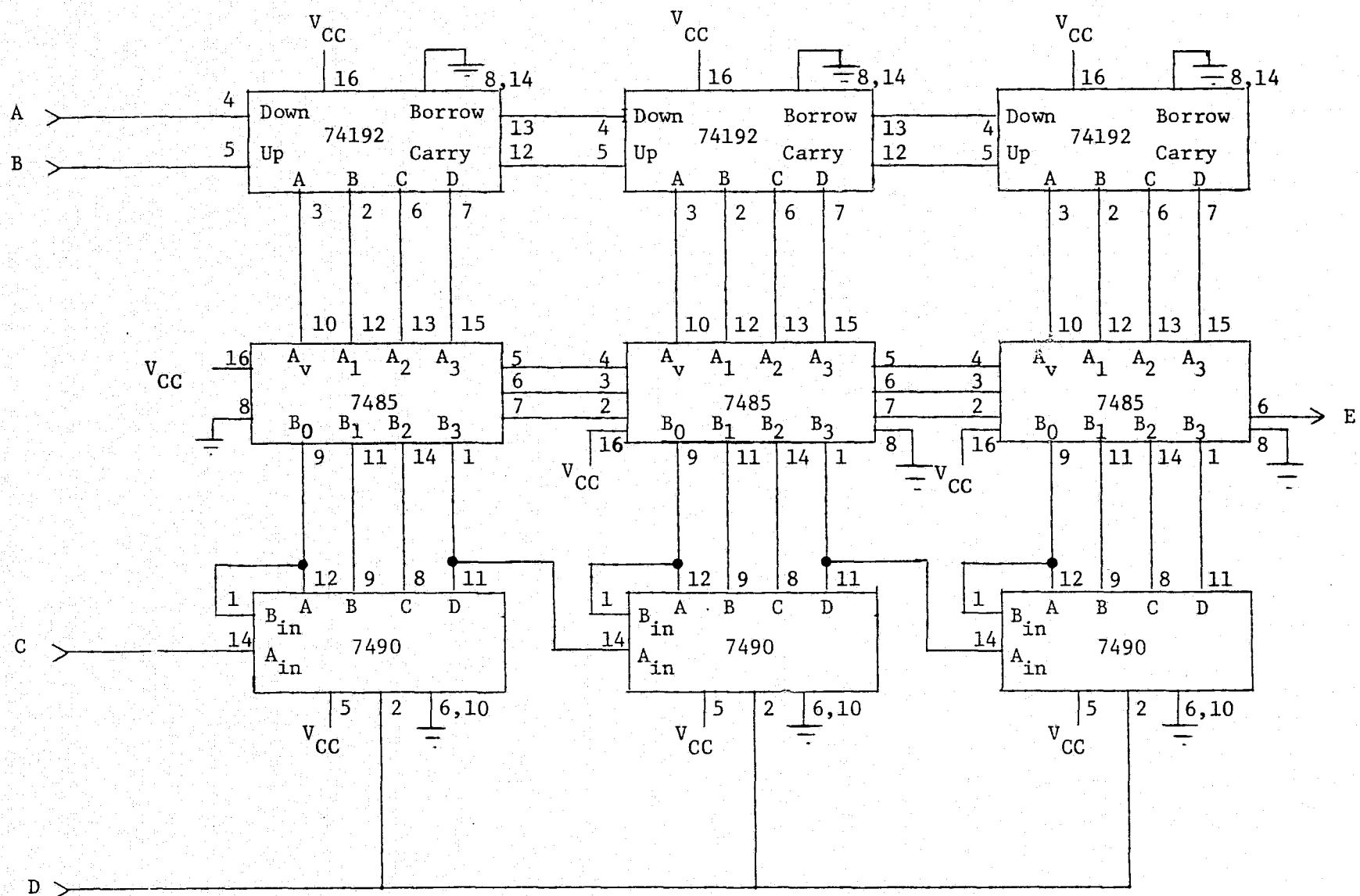


Figure 4.12. Counter module.

is again zero. This same delay controls the phase position of the generated 2.5 KHz square wave.

In Figure 4.11 flip-flop A1 is triggered on the fall of the 2.5 KHz reference. The 2.5 MHz pulses, derived from the 10 MHz reference through dual flip-flops A2 are gated through A3 to C of the 1000-bit, slave counter. When the counts match, the counter module output E goes high. This signal and Q of A1 are gated to monostable multivibrators A4, A5, A6. A4 with a time constant of 100 ns clears A1 and resets the 1000-bit counter. A5 closes the gate Q1, through comparator A8, to the synchronous detector A10 for 200 μ sec, or 0.5 period of the reference wave. A6 is triggered with a pulse width of 100 μ s, which is 0.25 periods of 2.5 KHz, or 90°. Then A7 is triggered and has a time constant of 200 μ s. One gate of A3 is used as a line driver to route the 2.5 KHz reference to the output synchronous detector.

Before the next falling edge of the 2.5 KHz reference triggers A1, A5 returns to the low state. This opens gate Q1 through comparator A8. The signal is applied to detector A10 through buffer amplifier A9 and gate Q1. If the gate and signal are not 90° out of phase, the detector A10 will produce an output, positive or negative. For the positive output, comparator A11 output goes negative. This sets gates A12 such that the output of the monostable multivibrator A13 is routed to the "down" input of the up-down counter. A negative output of detector A10 routes A13 output to the "up" input. Therefore the slave counter will require a lesser or greater number of counts to match the up-down counter registration. Then the phase at which A5 triggers will be advanced or retarded and this will result in a similar phase change of the gate signal on Q1. The circuit continues to cycle until

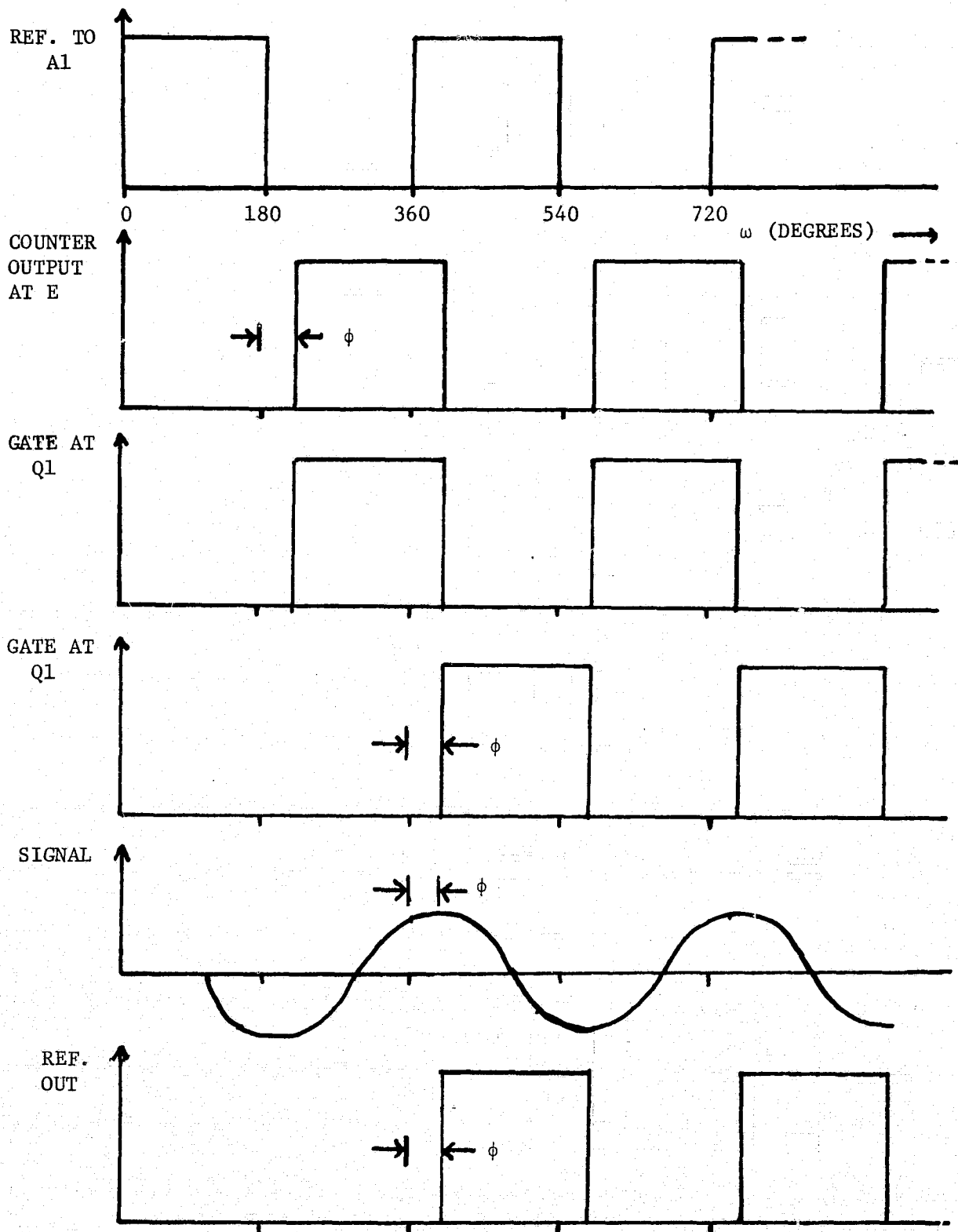


Figure 4.13. Signal phase positions in the locked state.

the output of A10 is zero volts, which means the gate signal on Q1 and the input signal are 90° out of phase.

The count rate of the up-down counter is obtained from A13 which has as its input source $1/2$ multiple of 2.5 KHz from one of the outputs of A14 through A20.

Figure 4.13 shows the relative phase positions of various signals when lock is acquired. Multivibrator A1 triggers at 180° and counter module output E goes positive after an inherent circuit delay, ϕ . A5 is triggered and holds gate Q1 closed for 180° . The gate Q1 is opened at $360^\circ + \phi$, i.e., at circuit delay ϕ . Then lock condition requires that the input signal be positioned at $\phi + 90^\circ$. The positive output from the counter module at E also initiates the generation of the reference output, shifted by 90° . Therefore the reference output is also positioned at $\phi + 90^\circ$.

Figure 4.14 shows the phase lock loop circuit with device identifications and component values. The 2.5 MHz rate provides 1000 bits per period of the 2.5 KHz reference. Each reference period is divided into $360/100$ or 0.36 degrees per count. The 3.9 Hz rate to the up-down counter is being used. Therefore phase correction occurs at 3.9×0.36 or 1.4 degrees per second. The up-down counter moves such that 180° of phase connection is the maximum ever required. Therefore maximum capture time is $180/1.4$ or 128.6 seconds. The 3.9 Hz rate was elected to minimize overshoot of lock position and jitter in the locked condition. The circuit is very stable and, if necessary, it could be operated with a higher frequency to the up-down counter.

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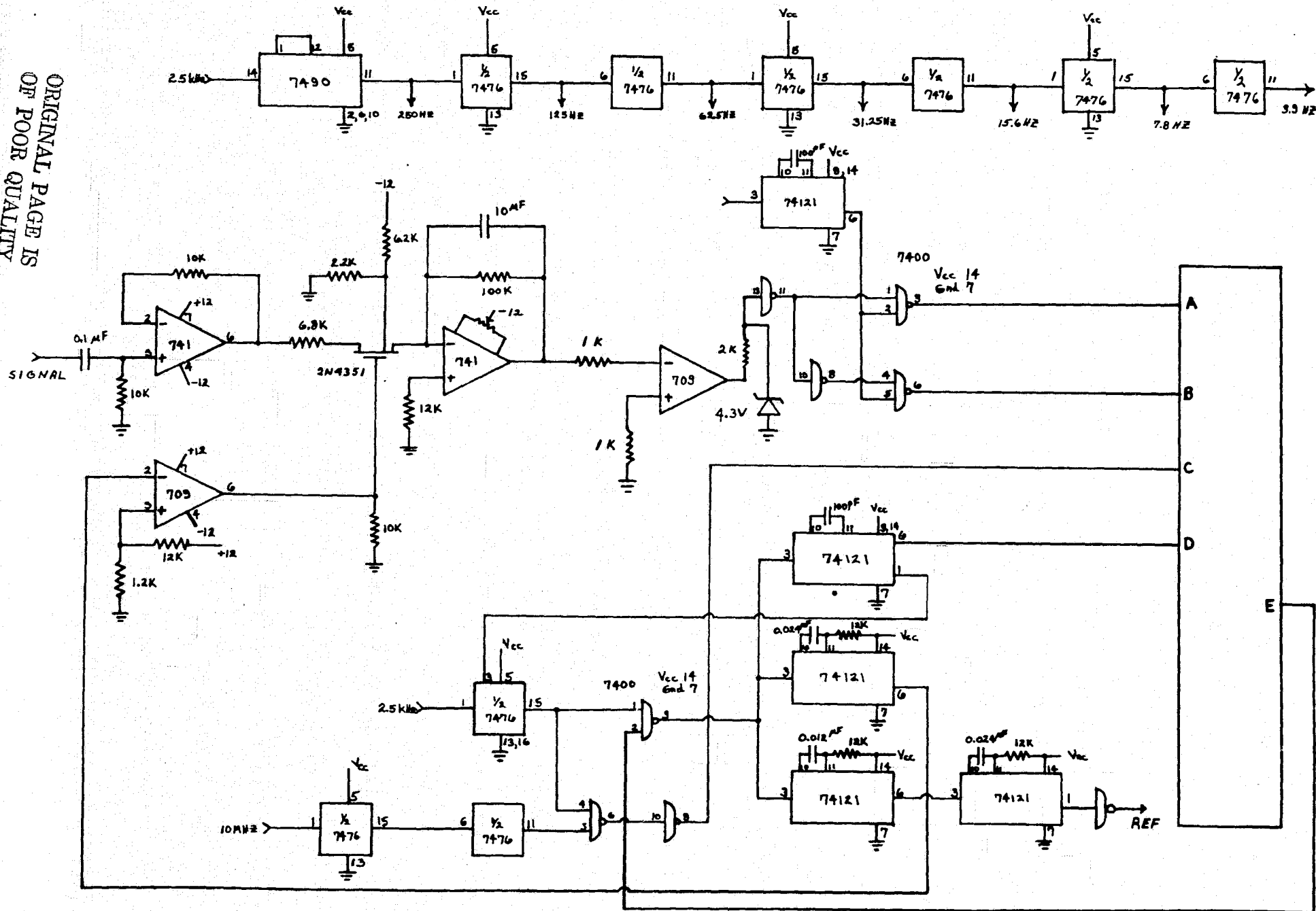


Figure 4.14. Phase locked loop circuit with component values shown.

4.2.7 Four Quadrant Phase Detector

The phase relation between the co-polarized and cross-polarized signals is to be investigated in the CTS experiment. Changes in phase may exceed 90° and therefore the conventional phase detectors may not be adequate. Also, the analog signals involved are normally too small for reliable operation of conventional phase measuring circuits.

The phase-lock loop described in the previous section shifts the 2.5 KHz reference square wave until it is in phase with the cross-polarized signal. Of course, the 2.5 KHz reference square wave is in phase with the co-polarized signal as a result of the co-polarized channel phase lock. Therefore phase can be measured accurately with the circuit of Figure 4.15.

The reference square wave from the co-polarized channel is used as input 1 to the flip-flop (7476). Input 2 is the shifted reference square wave from the 2.5 KHz phase-lock loop in the cross channel. The flip-flop triggers on the trailing edge. Therefore its output is a rectangular pulse proportional to the phase difference between the co and cross signals. The operational amplifier circuit is an integrator which produces a DC voltage, from the flip-flop output, proportional to phase difference between the co and cross signals.

The phase detector is calibrated by grounding test point A with signals removed. The detector output will reach a maximum value. With no signals applied and test point B grounded, the detector output will reach a minimum value. The 0° to 360° phase range is represented by the linear voltage range between the minimum and maximum voltage output of the detector. These levels were 0.06 V and 4.23 V for the unit installed in the CTS IF signal processor.

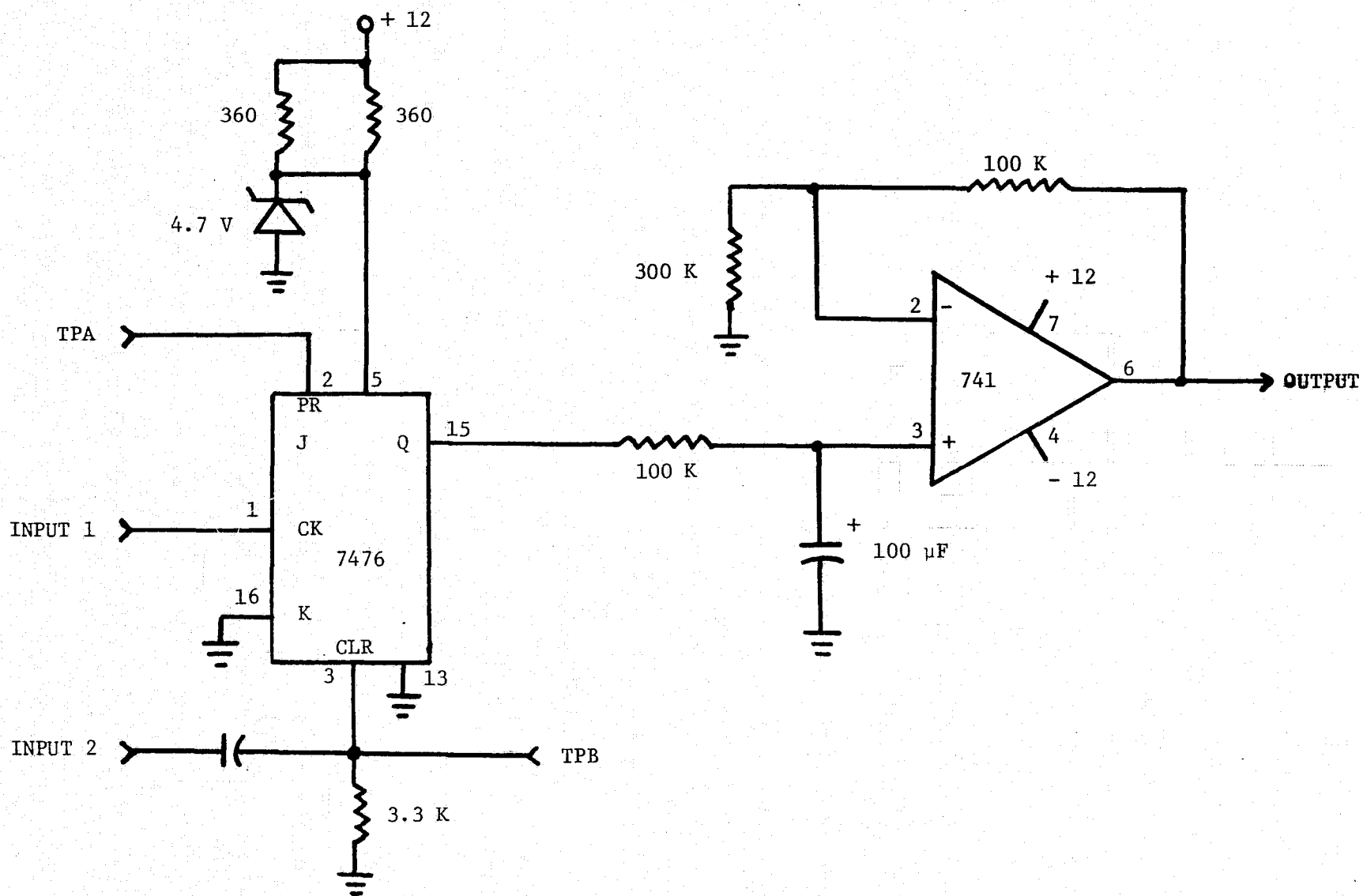


Figure 4.15, Four Quadrant Phase Detector

4.3 IF System Performance

All of the circuits described in the previous section have been installed and are operating in the VPI&SU CTS IF receiver. The improvement in performance is dramatic. The original Martin-Marietta ATS-5 receiver had a dynamic range of less than 25 dB and required a SNR of +20 dB (referenced to a 10 Hz bandwidth) in order to maintain phase lock. In addition, the sweep and phase locking circuits were inherently unstable and required frequent adjustment. Most of the time an SNR greater than 20 dB was required to maintain lock. With the installation of the new VCXO filter, sweep, and bandwidth control circuit, the receiver would maintain phase lock with an SNR of about 0 dB. However, this extra 20 dB of sensitivity was not usable since the signal was below the threshold of the original detector. In addition, a 0 dB SNR made the signal virtually indistinguishable from the noise and therefore useless.

The synchronous detector was added next in an effort to use this additional 20 dB of sensitivity. The synchronous detector provides an equivalent bandwidth of 0.016 Hz compared to a bandwidth (predetection) of about 75 Hz for the unmodified receiver. This reduction in bandwidth produces a 36.7 dB improvement in the SNR at the detector output. The system was then limited once again by the sensitivity of the phase locking circuitry. The synchronous detector is followed by a new logarithmic amplifier with a dynamic range in excess of 60 dB. Since the detector has no threshold, the dynamic range of the receiver can be in excess of 60 dB. In practice, however, it is limited at the lower end by the loss of phase lock due to the presence of noise.

The phase locking sensitivity of the cross-polarized receiver has been

improved by about 20 dB by the addition of the 2.5 KHz phase locked loop. As a result the dynamic range of the cross-polarized receiver is nearly that of the logarithmic amplifier.

The best indication of the actual operation of the CTS IF receiver system can be obtained from the calibration curves shown in Figure 4.16. The co-polarized receiver saturates at about -71.3 dBm and will maintain lock down to -110.6 dBm. The usable dynamic range is 39.3 dB. The cross-polarized receiver saturates at about -50 dBm and will maintain lock (with measureable signal output) down to -105.1 dBm. The usable dynamic range is 55.1 dB.

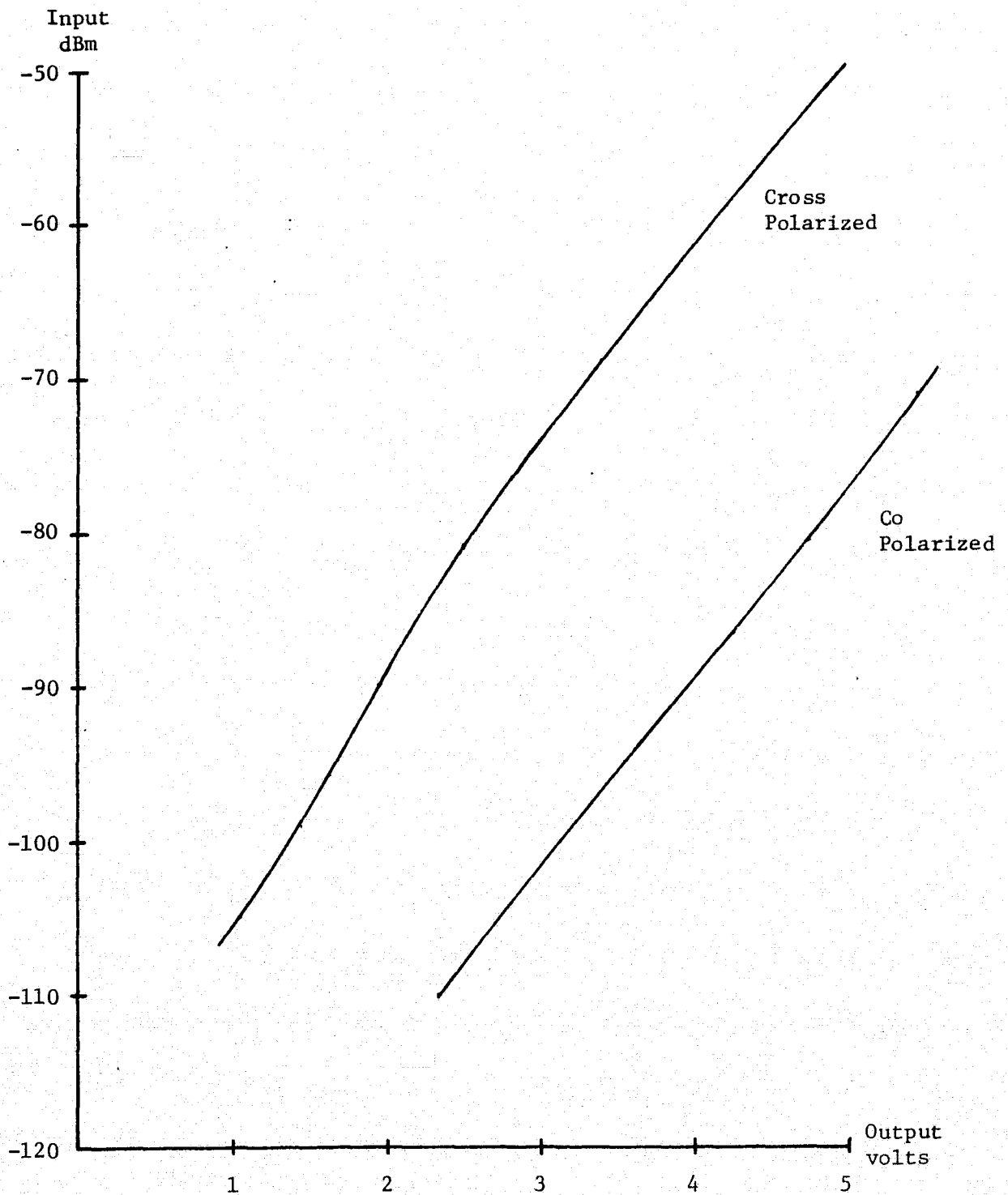


Figure 4.16. CTS IF Receiver Calibration Curves

5. Data Collection and Processing

5.1 Data Acquisition and Control System

The data acquisition and control system for the VPI&SU CTS experiment consists of an experiment controller and a mini-computer. This system controls the experiment, records data, and provides information about the overall status of the experiment.

The controller performs three main functions: (1) interfacing the computer to the rest of the experiment, (2) providing a system clock and event timer, and (3) converting analog signals to digital form. Its operation is relatively simple. The controller scans its 32 input channels looking for an input indicating an interrupt status. This interrupt status can come from an external event such as a rain gauge trip or from the timing section of the controller when it determines that the time has come to sample a particular input. When an interrupt occurs, the controller converts the analog data to digital, joins with it the date and time along with a data identifying number, and interrupts the computer. The computer then accepts the data.

Another important function of the controller is to take data from the computer and give it to another device, for example passing a new azimuth to the antenna pedestal. The controller can also be used by the computer to generate a control signal to operate a relay and control some external function. One such function is the initiation of an automatic test of all rain gauge telephone lines each midnight.

Physically, the controller is constructed on a wire-wrap type board which lends itself to whatever changes may be necessary to accomodate new equipment. It contains over 200 TTL integrated circuits in addition to the analog to digital converter and multiplexers. The controller is connected to the

computer by five 50 wire cables.

The mini-computer used in the project is a digital equipment corporation PDP 11/10. It has 32K bytes of core memory and a disk drive with a capacity of 2.4 mega-bytes. Serial input-output ports are used for the system console, remote logger, CRT terminal, and a modem. In addition to these the system has dual cassette tape drives which are used mainly during system generation.

The PDP-11 operating system is the RT-11 single job monitor system. This is the small single job version of RT-11 which does not provide any real time services. This version was chosen because it has a low core storage requirement and the controller already provides the basic timing necessary to drive the operational program. RT-11 provides a macro assembler, Fortran IV compiler, linker, and file editor. Utility programs have the capability to generate object libraries, and copy, rename, delete, or compare files in the system. At the present time, no other use can be made of the PDP 11 system while the operational program is running. Consideration is being given to using another version of RT-11 which would allow another job to run concurrently with the operational program when more core storage is added to the system.

Most of the operational program is written in Fortran but certain specialized routines are written in assembly language. The current program exceeds the available core storage and is put into overlays to save space. The routines which are in overlays are read in from disk to core as needed. This gives a nearly unlimited expansion capability for the part of the program which does not have to stay core resident. The operational program has three main parts; the interrupt processor, the task dispatcher, and the service routines called by the task dispatcher.

The interrupt service routine for the experiment controller is written in assembly language. It is entered automatically by the PDP 11 hardware whenever the controller has data for the program. This routine interacts with the controller to move the data into core storage and then calls a Fortran routine to process the data. If the data identification number corresponds to an analog signal such as a receiver output, the data is tested for a significant change since the last recorded point and put in a data queue to be recorded on the disk if appropriate. A rain gauge trip is placed in this queue when detected. Some data ID numbers are used as interval timers. When they are received, various status indicators are tested and possible tasks queued. For example, when the 10 minute interrupt comes an element is placed in the task queue to initiate the routine which points the antenna. After processing is completed by the Fortran routine, a return is made to the assembly language interrupt routine which in turn returns to where ever the program was when the controller called the routine.

The heart of the operational program is a repeated call to the task dispatching routine. The task dispatching routine is called from most of the task performing routines that it itself calls and therefore is written in assembly language to allow it to be re-entrant. The job of the task dispatcher is to check for commands from the PDP 11 switch register, see that all data in the data queue are written on the disk, and to select and execute tasks from the task queue. Each task is given a priority when it is entered in the queue, and a task is selected for execution only when it has a priority higher than the routine which called the task dispatcher. This allows the tasks which print reports to finish before another task is started unless the other task has a higher priority. An example of this is pointing

the antenna to zenith in case of high winds. This task has the highest priority of all and any other task will be interrupted to allow this to take place.

The routines called by the task dispatcher make up the bulk of the operational program. These are called in response to the interrupt processing part of the program or on a command given by someone placing a switch up on the PDP 11 console. Each routine must call the task dispatcher frequently to allow tasks of higher priority to execute. Under a real time operating system, the task dispatcher itself could be made a task of the operating system and the explicit calls to it would not be necessary.

At the present time routines exist to perform the following functions:

- 1) Print daily report.
- 2) Print last 50 recorded data points.
- 3) Print status report.
- 4) Test rain gauges.
- 5) Print rain rate report.
- 6) Point antenna.
- 7) Warn of receivers in test mode.

At ten minute intervals, the antenna is pointed and the pointing logged on the remote logger. If the receivers are in test mode, this fact is also logged. An hourly status report is printed by the logger giving statistics on the current data values, the amount of data taken, as well as when the operational program was last started and the present outside temperature.

Table 5.1 Summarizes the Data Presently taken by the System

Table 5.1
Experiment Data

Co-Polar Carrier	Sample Rate Resolution Dynamic Range Source	1/Sec 8 Bits 39 dB Receiver 1
Co-Polar Carrier	Sample Rate Resolution Dynamic Range Source	10/Sec 8 Bits 39 dB Receiver 1
Cross-Polar Carrier	Sample Rate Resolution Dynamic Range Source	1/Sec 8 Bits 55 dB Receiver 2
Cross-Polar Carrier	Sample Rate Resolution Dynamic Range Source	10/Sec 8 Bits 55 dB Receiver 2
Phase	Sample Rate Resolution Dynamic Range Source	1/Sec 8 Bits 0 = 360 Deg. Receivers 1 & 2
Rain Rate	Resolution Source	Time to 1/5 Sec 5 Gauges
Wind Speed	Sample Rate Resolution Dynamic Range Source	1/ (4 sec) 8 Bits 0 = 60 MPH 2 Sensors
Wind Direction	Sample Rate Resolution Dynamic Range Source	1/ (4 Sec) 8 Bits 0 = 260 Deg. 2 Sensors
Outside Temperature	Sample Rate Resolution Dynamic Range Source	1/ (10 Min) 8 Bits -35 C to 55 C 1 Sensor
Status	Receiver 1 Phase Lock Receiver 2 Phase Lock Receiver Test Mode Pedestal Malfunction Antenna to Zenith	

5.2 Data Reduction

During periods of low experimental activity, the operational software may be halted for accumulated experimental data transmittal to a central IBM 370 computer. Data are transferred to the IBM system via CMS (Conversational Monitor System) using a set of special communication programs developed especially for this purpose. Initially the connection to CMS is established using a standard data communications terminal. The CMS program to receive the data is then readied. Next, the PDP-11 program to transmit the data is readied. The communication link to CMS is then connected directly to the PDP-11 and the data transmission begins. Considerable care has been taken to make the software used in the data transmission as secure and self sustaining as possible. Virtually any transmission error can be detected and subsequent recovery is automatic. Both programs maintain written logs of errors and other parameters during the transmission. Additionally, the PDP-11 periodically writes a message on the logger in Whittemore Hall indicating the progress of the transmission. When the transmission is complete, the PDP-11 automatically logs itself off the time sharing system. Manual intervention is then required to restart the operational software.

After transmission the data reside on a CMS disk file and are formatted for convenient editing to correct errors. These errors usually arise from data being collected without proper initialization of the PDP-11 time and date and are not the result of software or hardware problems. The standard CMS text editor is employed to perform the editing. When the accuracy of the file has been verified, a batch job stream is generated from standard job control language and the transmitted data. This batch job makes use of a program stored on on-line disk to copy the data contained in the job stream

to tape. Two identical tapes are maintained and each tape is generated from the same job stream, submitted twice, with appropriate JCL changes. Thus, two permanent copies of the experimental database are produced. In the event one tape is lost or destroyed, the other can be used. Each tape is generated in a separate job to prevent both tape volumes from being mounted simultaneously and thus being simultaneously vulnerable. During this copy operation, the calibration curves for the two CTS receivers are applied to the signal data points. The resulting tape signal data is in absolute form and no longer requires a calibration curve to be meaningful.

Tape data processing is performed in two independent steps. A batch program stored on on-line disk is employed to select a section of the tape to be processed. This selection is made by specifying the starting and ending dates and times of the desired data. The program extracts the nearest proper subset of the data corresponding to the specified interval and generates what is referred to as a "process file." This file is the tape data expanded into a time history with rain rate computations performed and all weather and other experiment calibrations applied. It resides on on-line disk until another file is generated to replace it and thus may be accessed by a variety of analysis program running independently of one another. The use of this process file technique has three principal advantages. First, it minimizes the number of times a given section of the tape file must be processed. Second, it makes a very large database easy to manage. Third, the analysis programs can be simplified greatly due to the processing that was performed as the file was generated. Additionally, the process file generation program produces listings indicating the amount and type of data processed and can optionally produce a formatted dump of the generated time history.

Various Fortran routines have been written to generate plots from the process file. They display signal levels, isolation, attenuation, relative phase, and rain rate versus time and versus each other.

6. System Performance

Table 6.1 gives the link power budget between the satellite and the VPI&SU earth station. The -113.0 dBm power available from the antenna neglects any polarization mismatch between the wave and the antenna. By rotating the antenna feed (see Section 2.3) the co polarized output is maximized and cross polarized output is minimized. Then in Channel 1 (co-polarized) there is essentially no polarization mismatch. In Channel 2 (cross-polarized) the output power from the antenna port typically 35 dB below that from the co-polarized port for a nominal 35 dB isolation. The receiver power budget for both channels is presented in Table 6.2 The waveguide losses are estimated. The RF to IF gains were measured by LNR. The coaxial cable loss was measured. Using the IF calibration system the satellite signal power to the IF processor in Channel 1 was measured to be -80.3 dBm. Thus the difference between expected and actual power levels is $-77.9 - (-80.3) = 2.4$ dB.

Table 6.1

CTS Spacecraft to Blacksburg Ground Station

Signal Power Budget

1.	Frequency (cw)	11.700 GHz
2.	Transmitter power (minimum, primary)	200 mW 23.0 dBm
3.	S/C antenna gain	19.6 dB
4.	EIRP	42.6 dBm
5.	Path loss	205.5 dB
6.	Clear sky attenuation	0.3 dB
7.	Off-axis pointing losses	0.6 dB
8.	Net losses	206.4 dB
9.	Ground station antenna gain (measured by S-A)	50.85 dB
10.	Power available from antenna output flanges	-112.95 dBm

Table 6.2

CTS Blacksburg Ground Station Receiver Performance

	Ch. 1 <u>Co-Polarized</u>	Ch. 2 <u>Cross-Polarized</u>
Power level at input to antenna feed	-113.0 dBm	-148.0 dBm
Waveguide loss	0.4 dB	0.4 dB
RF to IF gain	41.5 dB	79.0 dB
Coax loss	6.0 dB	6.0 dB
Net RF to IF gain	35.1 dB	72.6 dB
Signal Power IF Processor	-77.9 dBm	-75.4 dBm
Noise temperature at antenna feed (including 20°K antenna temperature)	1102.2°K	228.2°K
Noise power at antenna feed, kTB, assuming B = 10 Hz	-158.2 dBm	-165.0 dBm
Noise power at input to IF signal processor, G(RF to IF) kTB	-123.1 dBm	-92.4 dBm
Signal-to-noise ratio	45.2 dB	17.0 dB

Note: The cross-polarized signal is assumed to be 35 dB below the co-polarized signal.